JPL D-13277, Rev C

# RISK/RELIABILITY MANAGEMENT GUIDELINE FOR DEEP SPACE ROBOTIC APPLICATIONS MISSIONS

Prepared by the Reliability Engineering Office of
the Office of Engineering and Mission Assurance

July, 1996

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California 91109

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# RISK/REQUIREMENTS TRADE-OFF GUIDELINES
## FOR FASTER, BETTER, CHEAPER MISSIONS

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**July, 1996**

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# PREFACE

This document is a compendium of Risk/Requirements Tradeoff Guidelines for Faster, Better, Cheaper missions. It summarizes the reduced-cost approach for the design, verification, and validation of flight equipment for assuring mission success of microspacecraft.

The first and second editions (Rev. A and B) of the document contained guidelines for a subset of product assurance activities that have been deemed critical in a recent study to prioritize them. This third edition (Rev. C) of the document contains more product-assurance guidelines from the prioritized list. Additional guidelines, not included in this revised document, will be included in future revisions. These guidelines are self-optimized in the parameters to whose variance they are sensitive. In order for the entire product assurance program to be optimized, the guidelines need to be optimized with respect to each other. Optimization between related disciplines (e.g. dynamic, thermal, analysis, etc.) will be made from existing guidelines in the next revisions. Subsequent revisions will involve optimization across disciplines and for combined disciplines. This document is intended to assist projects in their FBC effort, thus the guidelines will be periodically revised and updated to reflect the changing needs of future missions.

# DOCUMENT CHANGELOG

| REVISION | DATE | CHANGE DESCRIPTION | PREPARED BY |
|---|---|---|---|
| Rev. A | January 1996 | First Release | Reliability Technology Group, 505 (Kin F. Man, Editor) |
| Rev. B | April 1996 | Second Release | Reliability Technology Group, 505 (Kin F. Man, Editor) |
| Rev. C | July 1996 | Third Release | Reliability Technology Group, 505 (Kin F. Man, Editor) |

# ACKNOWLEDGMENTS

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This task is under the leadership of Dr. Steven L. Cornford, Program Element Manager of Payload Assurance in the Assurance Technology Program Office and Supervisor of the Reliability Technology Group in 505. This document is the product of the efforts of a number of personnel within the Office of Engineering and Mission Assurance, including Reliability Engineering, Quality Assurance, and Electronic Parts Engineering Offices. Each guideline may be the work of one or more contributors, whose efforts are greatly appreciated. The following table lists the primary author of each guideline, to whom detailed technical questions should be directed.

| Guideline | Primary Contributor |
|---|---|
| **Rev. A** | |
| 1. Acoustic Noise Requirement | Jim Newell |
| 2. Pyrotechnic shock Requirement | Jim Newell |
| 3. Radiation Design Margin Requirement | Michael Cherng |
| 4. Minimum Operating Time Requirement | Milena Krasich |
| 5. System-Level Fault Tree | John Koch |
| 6. Electronic Parts Stress Analysis | John Koch |
| 7. Unit Level Temperature Design Requirement | Tim Larson |
| **Rev. B** Additions | |
| 8. Unit Level Thermal Test Requirement | Mark Gibbel |
| 9. Electronics Parts Destructive Physical Analysis | Stephen James |
| 10. Quality Assurance Site Survey Requirement | Diane Sipes-Cwik |
| 11. Electrostatic Discharge Control Program Requirement | Kirk Olsen |
| **Rev. C** Additions | |
| 12. Spacecraft Grounding Requirement | Albert Whittlesey |
| 13. Flight Electronic Parts Inspection Requirement | Diane Sipes-Cwik |
| 14. Quality Assurance Plan Requirement | Diane Sipes-Cwik |
| 15. Manufacturing Process Review Requirement | Diane Sipes-Cwik |
| 16. Problem/Failure Process | John Koch |

Many of the authors have reviewed the guidelines. Valuable review comments were also provided by Phil Barela, Steve Cornford, Chuck Gonzalez, and Kin Man. in addition, Perry Danesh, Ken Erickson, Lynn Gresham, Jim Moldenhauer, Guy Spitale, and Al Whittlesey have taken part in (discussion meetings to generate valuable ideas for this task.

The editor is responsible for any remaining errors and welcomes comments and suggestions for improvement to its usefulness. Questions or comments should be directed to Dr. Kin H. Man, at (818) 393-0255.

# CONTENTS

# INTRODUCTION

As the trend towards Faster, Better, Cheaper missions accelerates, it presents managers and project personnel with additional challenges of devising streamlined guidelines for implementing this new way of doing business. '1'bus, there is a renewed emphasis on tradeoffs bet ween requirements and risk to reduce cost, while still improving quality, reliability, and schedule, The risk/requirements tradeoff guidelines contained in this document arc intended to assist projects in this endeavor. The objectives of these guidelines can be summarized generically as: to 1 ) demonstrate operation in a filglIt-like environment; 2) validate. design; 3) demonstrate robustness; 4) detect workmanship flaws; and 5) demonstrate reliability. Each guideline addresses one or more of these objectives. The definition of these objectives, as used in the context of our task, are defined in greater detail below:

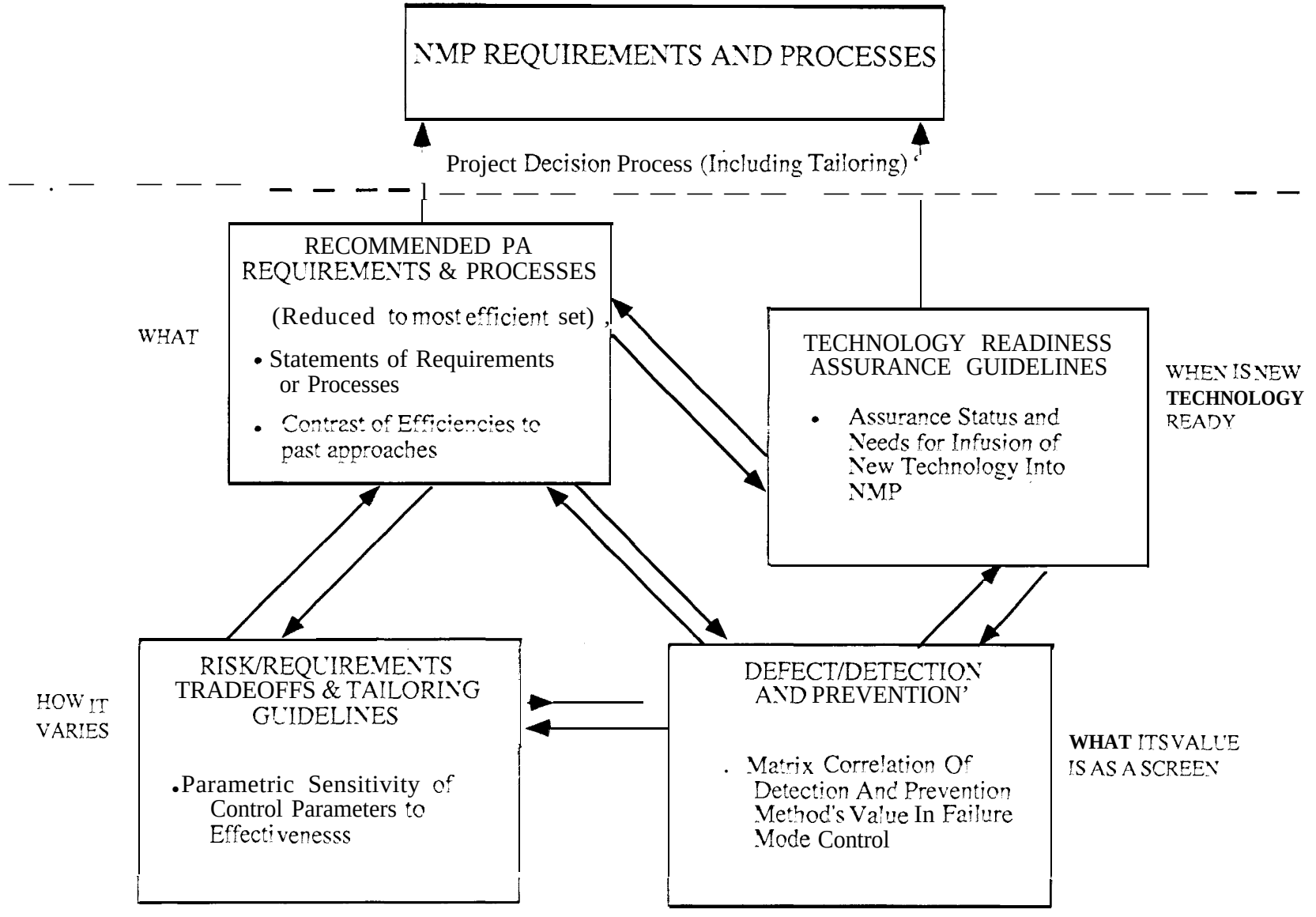
1. Demonstrate operation in a flight-like environment - demonstrate hardware operation to design levels in a fright-like environment in which several operational parameters may interact synergistically with each other and with the test environment.
2. Validate design ---- demonstrate the ability of the electrical and/or mechanical hardware design to function within specifications in various operational modes (on/off cycles, start-up performance, deployment times, end-of-life conditions, etc.) and anticipated environments.
3. ] Demonstrate robustness - demonstrate. the ability of a unit to operate at levels beyond the expected flight/use environment, in order to quantify the various margins within a design. Testing to the limits of performance should not physically break or cause irreversible degradation or damage. Robustness demonstration typically involves electrical, mechanical, and thermal margins (e.g. sensitivity to voltage, clock frequencies, packaging design performance, thermal degradation, structural integrity, etc.).
4. Detect workmanship flaws - detect workmanship flaws that can cause time-dependent degradation to electrical and mechanical hardware, as well as non-time dependent failures. Workmanship flaws can result both from process variations in assembly ant] integration, and those that escaped from lower-lcvc] manufacturing operations.
5, Demonstrate reliability --- demonstrate the ability of the flight hardware to operate the required frictions under specified conditions for a stated period of time. Sufficient operating time is accumulated through testing to eliminate "infant-mortality" defects and to provide a measure of t] ie expected failure rate.

Each guideline focuses on a PACT (Prevention, Analysis, Control or Test) typically used to screen for specific potential failure modes. A list of predominant failure modes relevant to each guideline is also generated , In most cases t hey are supported by result S Of searches from ground test and in-flight problem/failure databases for JPL and GSFC flight missions. The significance of categories of failure modes to the achievement of overall mission success is addressed in terms of performance tradeoffs within the PACTs. Cost drivers in the performance of these specific PACTs are identified for potential tradeoff studies. Parametric tradeoffs that would be cost effective arc indicated. In addition, effective substitutes for specific PACTs are identified.

These guidelines are. the evolving product of the Risk/Requirements Tradeoff task. This task is part of a suite of four tasks in the New Millennium Mission Assurance Project Applications RTOP, sponsored by the l'ayloads/Aeronautics 1 Division (QT) of the Office of Safet y and Mission Assurance (Code Q) at NASA. This suite of tasks is designed to function synergistically to enable the emerging needs of microspacecraft (p-S/(:) ant] to remove the roadblocks for achieving their goals (Figure 1). The first Of the four tasks, the Recommended Product Assurance R equirements and l'rote.sscs task, determines criteria for a minimum set of product assurance requirements to ensure mission success. It recommends a set of specific reliability, environmental, parts, and quality requirements for µ-S/C applications. For each of the issues identified in the first task, the second task, in the form of tradeoff and tailoring, guidelines, determines the impact on the risk of

increasing or reducing the parametric values of these requirements. These guidelines allow project managers and personnel to understand the issues involved in order to allow tradeoffs to be made. The failure modes generated for each requirement feed directly into the third task, Defect Detection and Prevention, which utilizes the Accurate, Cost-Effective Qualification (ACEQ) approach to systematically examine these failure modes with the mission requirements. This process results in a matrix of weighted influence coefficients. When combined with a plot of failure modes versus the PACTs, a ranked list of PACTs is generated from which project personnel can tailor the qualification program for a particular mission. The forth task, Technology Readiness Assurance Guidelines, identifies unknown effectiveness parameters, assesses the readiness of a new technology to be inserted into flight projects, and identifies focused research efforts into potential risk elements. This task provides the assurance status and need for infusion of new technologies into the New Millennium Program.

# NMP MISSION ASSURANCE PROJECT APPLICAITONS RTOP



# Guidelines

# 1. Acoustic Noise Requirement

## 1.0 Objectives

Acoustic noise results from the propagation of sound pressure waves through air or other media. During the launch of a rocket, such noise is generated by the release of high velocity engine exhaust gases, by the resonant motion of internal engine components, and by the aerodynamic flow field associated with high speed vehicle movement through the atmosphere.

The fluctuating pressures associated with acoustic energy can cause vibration of structural components over a broad frequency band, ranging from about 20 Hz to 10,000 Hz and above. Such high frequency vibration can lead to rapid structural fatigue. Thus, the objective of a spacecraft acoustic noise requirement is to ensure structural integrity of the vehicle and its components in the vibroacoustic environment.

## 2.0 Typical Requirement

A typical acoustic noise requirement is illustrated in Figure 1 below.

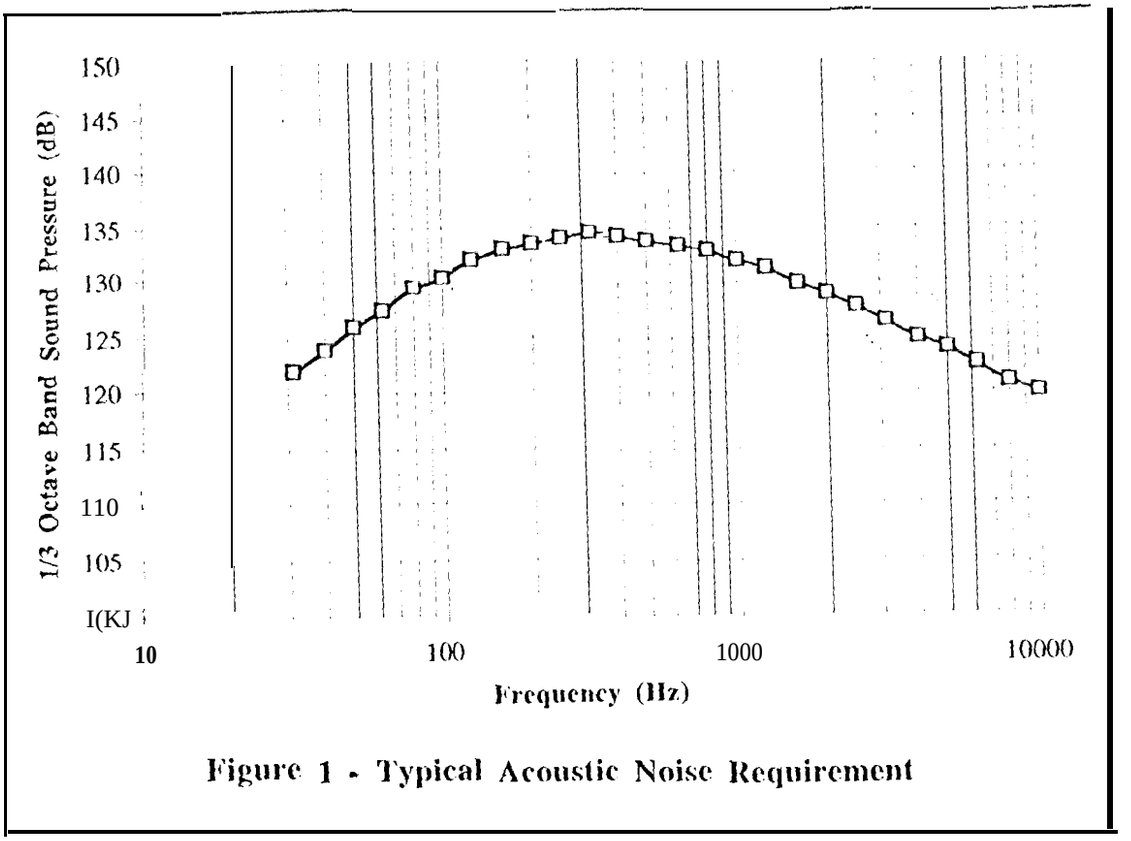



**Figure 1 - Typical Acoustic Noise Requirement**

Such a figure specifics the. level of input sound pressure over the spectrum of frequencies at which the pressure can fluctuate. The pressure 1' is measured in decibels, defined as

$$dB = 20 \log \frac{P}{P_{ref}}$$

where the reference pressure. $P_{ref} = 2 \times 10^{-5}$ Pa, ostensibly the audible limit of the human ear.

The decibel pressure levels in acoustic noise spectra are not generally provided at each and every frequency. Instead, they are often specific.d over discreet bands of width Af, which span 1/3 of a frequency octave. With this method, 3 sound pressure levels will be provided over any interval in which the frequency doubles. Table 1 is an example of such a 1/3 octave band specification, for the curve data of Figure 1.

**Table 1 - Acoustic Specification**

| Center Frequency | SPL ((m) |
|---|---|
| 31.5 | 122.0 |
| 4(LO | 124.0 |
| **50,0** | 12(1.0 |
| 63.0 | 127.5 |
| 80.0 | I 29.s |
| 100.0 | 130.5 |
| 125.0 | 132.0 |
| I 60.0 | 133.0 |
| ?00.0 | 133.5 |
| 250.0 | 134.0 |
| 315.0 | 134.5 |
| 400.0 | 134.5 |
| 500,0 | 134.0 |
| 630.0 | 133.5 |
| 800.0 | 133.0 |
| 1 000.0 | 1320 |
| 1250.0 | 131.5 |
| 1600.0 | 130.0 |
| 2000.() | 129,0 |
| **2500.0** | 128.0 |
| 3150.0 | 26.s |
| 4000.0 | 25.0 |
| 5000.0 | 24.0 |
| 6300.0 | 22,5 |
| 8000.0 | 21.0 |
| 10000.0 | **20s)** |

When pressure levels are defined with these methods, it is convenient to provide a measure of the overall acoustic noise intensity. The overall sound pressure level (OASPL) provides just such a measure and, for 1/3 octave band specifications, can be calculated as the decibel equivalent of the root sum square (RSS) pressure. Table 2 illustrates such a calculation for the data of Table 1, and shows that the OASPL is 144.9 dB. It should be noted that this figure is ~lc.ate) than any individual sound pressure level in the specification, because it represents an intensity of the spectrum as a whole.

'])'0 quantify the acoustic envir onment, launch vehicles are often equipped with internal microphones, which measure noise levels within the rocket fairing. This telemetry data is relayed to the ground for processing, and ultimately plotted in the form of a sound pressure level versus frequency spectrum. Since the acoustic forcing function is stochastic, depending on many atmospheric and other variables, data from a number of such flights are generally gathered, and an envelope, such as that of Figure 1, is (ic.vc.loped to encompass the historical record of microphone data.

This process can be extended and applied to data from a number of launch vehicles. If a launch platform has not yet been manifested for a particular payload, acoustic profiles from a number of candidate rockets can be enveloped, producing an aggressive specification which will ensure design adequacy for the spacecraft. Figure ? below reflects such a process, providing an envelope which encompasses the acoustic environments from three. launch vehicles.

**Table 2 - Calculation of Overall Sound Pressure Level**

| Center Frequency | SPL (dB) | Pressure J' (l%) | Squared Pressure |
|---|---|---|---|
| 31.5 | 127.0 | 25.? | 633.9 |
| 40.0 | 124.() | 31.7 | 1004.6 |
| 50.() | 126.0 | 39.9 | 1592.2 |
| 63.0 | 127.5 | 47.4 | 2249.1 |
| 80.0 | 129.5 | 59.7 | 3564.5 |
| 100.0 | 130.5 | 67.0 | 4487 S |
| 125.0 | 132.0 | 79.6 | 6338.7 |
| 160.0 | **133.0** | 89.3 | 7979.9 |
| 200.0 | **133.5** | 94.6 | 8953.6 |
| 250.0 | 134.0 | 100.2 | 10046.2 |
| 315.0 | 134.5 | 1 0 ( . 2 | 1 1272.() |
| 4(KI.O | 134.5 | 106.2 | 11272.0 |
| 500.0 | 134.0 | 100.2 | I 00.16.? |
| 630.0 | 133.5 | 94.6 | 8953.6 |
| 800.0 | 133.0 | 89.3 | 7979.9 |
| 1000.0 | 132.() | 79.6 | 6338.7 |
| 1?50.0 | 131.5 | 75,2 | 5649.4 |
| 1600.O | 130.0 | 63.2 | 3999.4 |
| 2000.0 | 129S1 | 56.4 | 3176.9 |
| 2500.0 | 128.0 | 50.? | 2523.5 |
| 3150.0 | 126.5 | 42.3 | 1786.5 |
| 4000.0 | 125.0 | 35.6 | 1?647 |
| 5000.0 | 124.() | 31.7 | 1 (KM.6 |
| 6300.0 | 122.5 | 26.7 | 711.2 |
| 8000.0 | 121.0 | 22.4 | 503.5 |
| 10000.0 | 120.0 | 20,0 | 399.9 |

**RSS Pressure = 351.8 Pa**
**20 log(351.8/2E-5) = 144.9 dB**

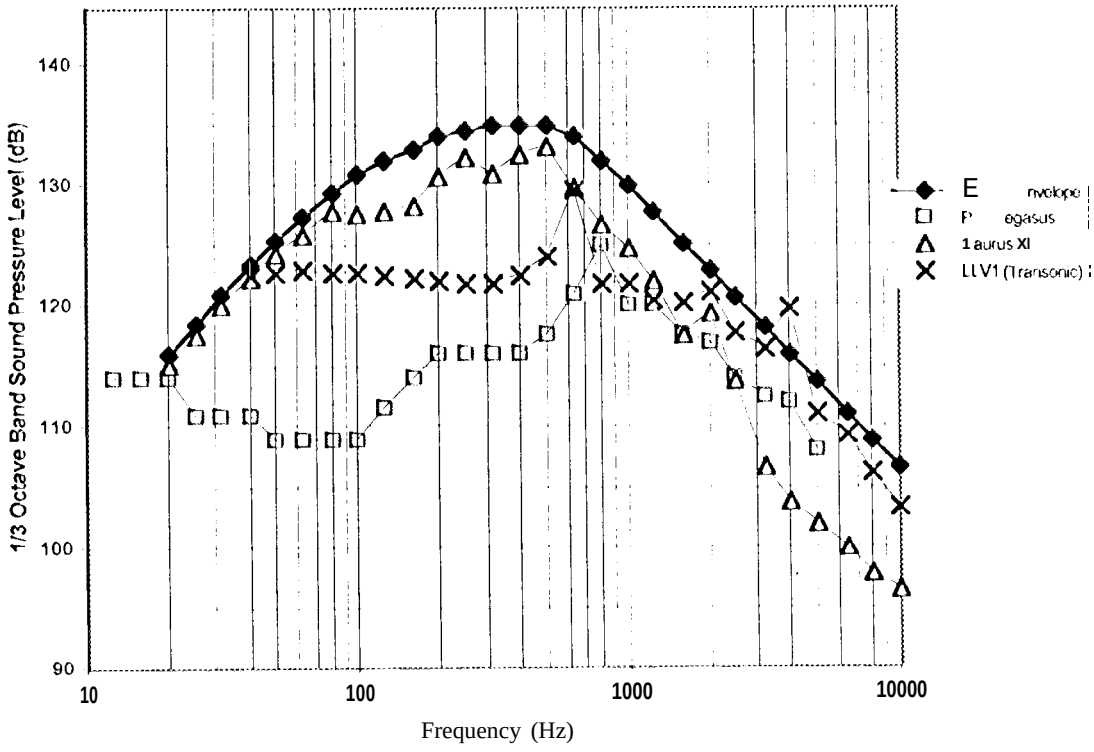



**Figure 2 - Envelope of Acoustic Flight Data**

## 2.1 Rationale

The rationale for acoustic noise testing is straightforward, as acoustic energy is the primary source of vibration input to a spare launch vehicle. During the initial phases of a rocket launch, high velocity gases are ejected from motor nozzles and reflected from the ground, creating turbulence in the surrounding air and inducing a vibratory response of the rocket structure. During the subsequent ascent phase of a launch, as the vehicle accelerates through the atmosphere to high velocity, aerodynamic turbulence induces pressure fluctuations which again cause structural vibration. These pressure fluctuations increase in severity as the vehicle approaches and passes through the speed Of sound, due to the development and instability Of local shock waves. The high-level acoustic noise. environment continues during supersonic flight, generally until the maximum dynamic pressure or "max Q" condition is reached.

Acoustic energy gets transmitted to the mission payload in two ways. First, fluctuating, pressures within the payload fairing impinge directly on exposed spacecraft surfaces, inducing vibration in high gain antennae, solar panels and other components having a large ratio of tile.:1-to-]lj:tss. Secondarily, the fluctuating external pressure field causes an oscillatory response of the rocket structure, which is ultimately transmitted through the. spacecraft attachment ring in the form of random vibration. From the space.mfl perspective, this random input is generally lowest at the launch vehicle attachment plane, and increases upward along the payload axis.

At the integrated spacecraft level, then, acoustic noise is a primary source of vibration excitation. It is a "real world" environment, and should be included in virtually any space vehicle test program.

### 2.1.1 Failure Modes

The failure mode.s produced by acoustic noise excitation are generally identical to those associated with other types of vibratory structural fatigue. These include failures due to excessive displacement, in which one deflecting component makes contact with another, as well as fractured structural members and loose fasteners. Broken solder joints, cracked PC boards and wave guides can also occur. Electronic components whose function depends on the motion of structural parts, such as relays and pressure switches, are particularly susceptible.

Large flat panels are most easily influenced by, and therefore damaged by, acoustic energy, as they can undergo large. displacements while oscillating at low frequency. For a typical spacecraft, this means that a fixed high gain antenna must be carefully designed and stiffened to avoid bending failures, debonding of composite members and related problems. In general, ally structure with a high ratio of surface area to mass can be expected to experience potential problems in the acoustic noise environment.

### 2.1.2 Supporting Data

Supporting, data for acoustic noise design, analysis and testing can be found in the references listed below, as well as in various launch vehicle user manuals. At JPL, the acoustic test has traditionally been severe, with the qualification environment generally established at 4dB above the expected launch noise profile. 'Table 3 provides a sampling of problems detected during acoustic tests on several major Laboratory programs.

| Table 3 - JPL Acoustic Test Problem/Failure History | | | |
|---|---|---|---|
| Program | Year | Subsystem | Failure Mode |
| Viking | 1973 | S/X Band Antenna | Cracked Epoxy |
| Viking | 1973 | S/X Band Antenna | Spacers Loosened |
| Viking | 1973 | S/X Band Antenna | Studs Loosened |
| Viking | 1973 | Infrared Mapper | Wire Shorted |
| Viking | 1973 | Radio Antenna | Screw Sheared |
| Voyager | 1977 | SIX Band Antenna | Magnetic Coil Debonded |
| Galileo | 1983 | Dust Detector | Sensor Cover Buckled |
| Mars Observer | 1991 | 1 elecom Subsystem | HGA Screws Backed Out |
| Mars Observer | 1991 | High Gain Antenna | HGA Struts Debonded |
| Mars Observer | 1991 | High Gain Antenna | Waveguide Broke |
| T o p e x | 1992 | Instrument Module | I/C Lead Wire Broke |
| Cassini | 1995 | High Gain Antenna | HGA Screws Backed Out |
| Cassini | 1995 | High Gain Antenna | IIGA Struts Debonded |

The testing has clearly identified improperly designed, underdesigned or undersized components. It is interesting 10 note that a majority of these problems have occurred in high gain antennas and related subsystems, which have the previously identified characteristics of large surface areas, low mass and bonded attachments.

## 3.0 Tradeoffs

Failure mode sensitivities and cost tradeoffs for the acoustic mist environment are illustrated in Figure 3 below. The primary test variables are acoustic noise input level, time duration for the test, frequency of noise. input and whether or not power is on in the test article.
Each test parameter in an acoustic noise trial is generally a cost drive.r. This is primarily due to the fact that the. text requires a large chamber, many support personnel and a significant amount of equipment,

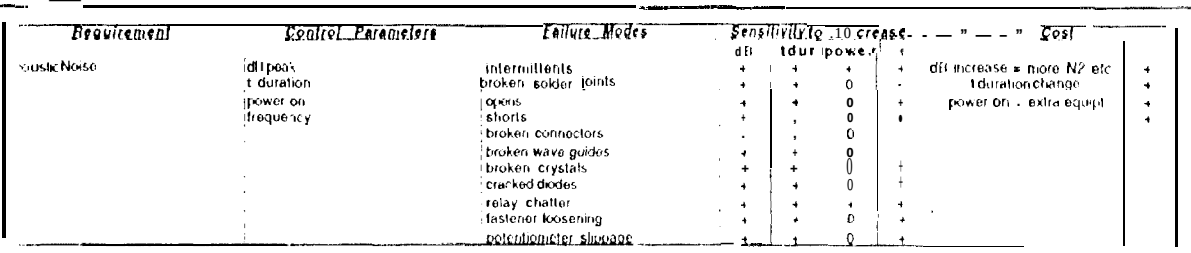



**Figure 3 - Control Parameter Sensitively and Cost**

## 4.() References


1. MIL-STD- 154(K, Test Requirements for Launch, Upper-Stage and Space Vehicles, United States Air Force Military Standard, 1994.
2. Steinberg, D. s., Vibration Analysis for Electronic Equipment, New York: John Wiley & sons, 1986.
3. 1 limelblau, 11., Fuller, C. and Scharton, 'J'., "Assessment of Space Vehicle. Aeroacoustic Vibration Prediction, Design and 'Jesting," NASA {3/-1596, July, 1970.

# 2. Pyrotechnic Shock Requirement

## 1.() Objectives

Pyrotechnic Shock is a design and test condition under which flight hardware is subjected to a rapid transfer of energy. The energy transfer is associated with the firing of an explosive device, usually for the purpose of initiating or performing a mechanical action. Spacecraft separat ion e vents or the release of propulsion system safing devices arc. typical of such mechanical actions.

## 2.0 Typical Requirement

A typical pyrotechnic shock requirement is illustrated in Figure 1 below.

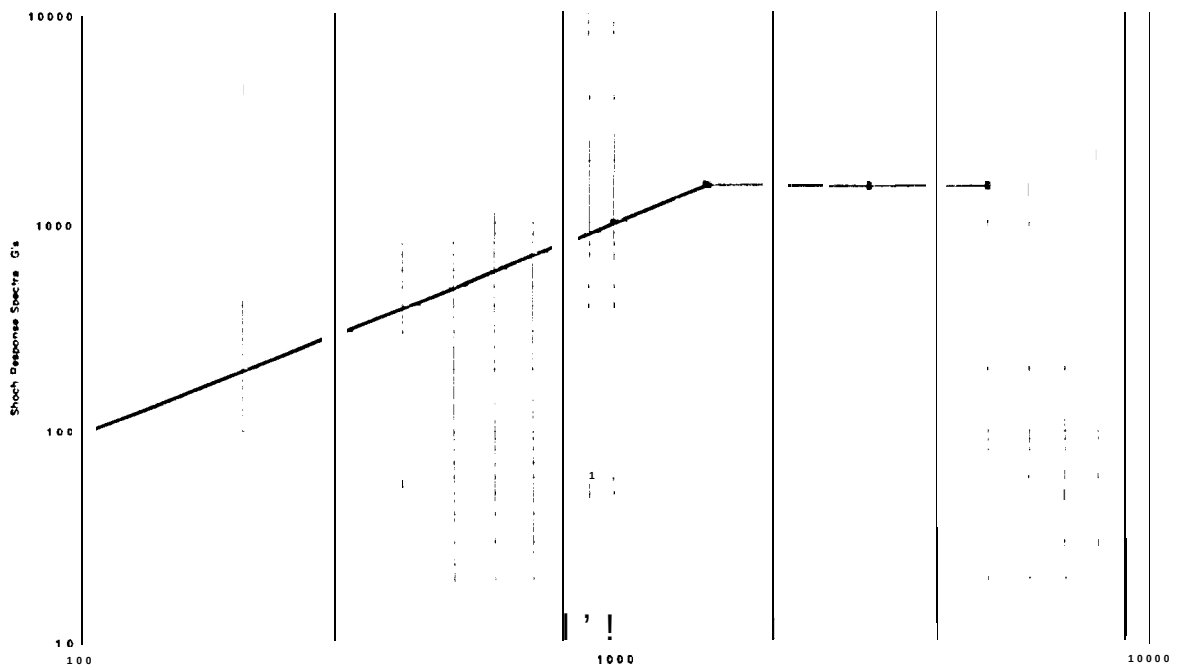



**Figure 1 - Typical Pyrotechnic Shock Requirement**

Such a figure gives the response of structure to the released shock energy, and illustrates a general trend that, as structural response frequency increases, the peak acceleration response increases as well.

## 2.1 Rationale

The release of energy from an ordnance-containing device and the subsequent transfer to surrou ndi ng struct ures represent a very complex event. As a result, it is difficult to describe the actual shape Of the applied shock wave; it is generally not a simple time-based pulse such as a square or triangular wave. 1 figure 2 illustrates a typical acceleration versus time. trace from an act ual pyrotechnic shock event.

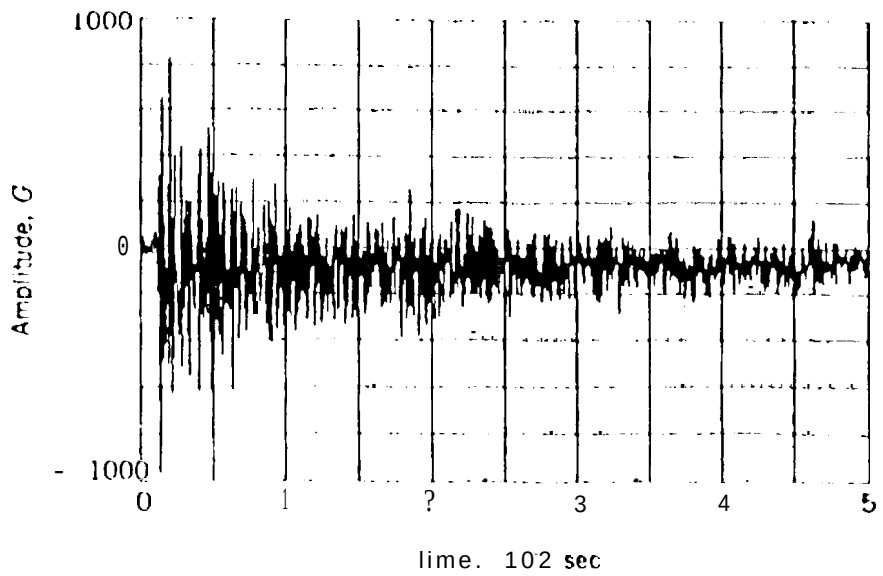



**Figure 2 - Pyro Shock Acceleration Time History**

Thus, in establishing a pym shock requirement, no attempt is made. to describe the input pulse, but the frequency-domain response. of the structure subjected to the pulse is described instead. Figure 3 below illustrates a typical measurement of this response.

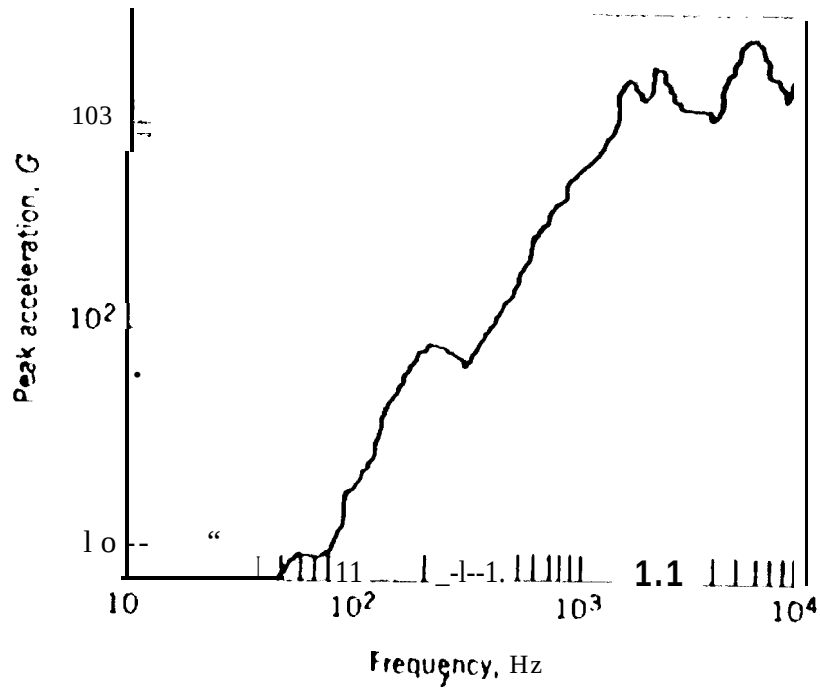



**Figure 3 - Frequency Response to Pyro Shock**

Obviously, the requirement shown in Figure 1 is derived from experience with some typical measurements shown here. The increase in peak acceleration with increasing frequency is a measured fact, and occurs because of the low effective mass generally associated with higher frequency structural resonances.

### 2.1.1 Failure Modes

The failure modes produced by shock excitation can be broadly grouped into four categories. First are those failures associated with high stresses, such as buckling of long and slender structures, plastic deformation of structures or fracture in brittle components. Next are failures due to high acceleration levels, which can cause relays to chatter, potentiometers to slip and bolts to loosen. 'Third arc problems associated with excessive displacement, which include broken solder joints, cracked PC boards and wave guides, or general problems associated with the impact of one structural component into another. The final category consists of transient electrical malfunctions, which occur only during application of the shock environment. Such malfunctions occur in capacitors, crystal oscillators and hybrids, the latter of which can temporarily short circuit during a shock event due to contact between the device package and internal die bond wires.

### 2.1.2 Supporting Data

Many studies regarding the effects of pyrotechnic shock have been conducted during the life span of the aerospace industry, but one of the best is perhaps that provided in Reference 1. Conducted by the Aerospace Corporation under contract to the Air Force Systems Command Space Division, the study examined and summarized ordnance-related shock failures over a period spanning some 20 years, dating from the first missile-related pyro shock failures in the early 1960s to about 1982 when the study was concluded. A total of 85 flight failure events are summarized in the paper, reflecting events ranging from relay chatter, broken electrical wires and leads, cracked glass diodes or fracture of brittle ceramic components and a number of others.

## 3.0 Tradeoffs

Failure mode sensitivities and cost tradeoffs for the pyrotechnic shock environment need to be discussed in the context of a particular test technique. The three principal methods for shock testing include shaker synthesis, resonant plate testing and actual firing of pyro devices.

In the shaker synthesis technique, the article to be shock tested is mounted to an electrodynamic vibration shaker using an appropriate fixture. A function generator is connected to the shaker, and a triangular, square wave, half-sine or similar time-based pulse is input to the test article in an attempt to generate the desired frequency response spectrum.

Generally, this is a trouble-prone and ineffective exercise because, as stated above, a pyro shock pulse rarely manifests itself as a simple function. Furthermore, the shaker synthesis technique tends to input excessive energy to the structure at low frequencies and insufficient energy at high frequencies. As a result, hardware subjected to such tests is often overtested in the low frequency regime and undertested elsewhere.

In an attempt to improve upon the synthesis method, many environmental test engineers have attempted to modify the input to the shaker using so-called "chirp" techniques. In this case, output from the function generator is passed through a graphic equalizer before being routed to the shaker. The shaker input spectrum is then "tuned" through an increase in the gain of high frequency signals, and through an attendant gain reduction at low frequencies. Unfortunately, such efforts offer marginal improvements at best, due to the inherent low-pass filter characteristics of a mechanical shaker.

in the. resonant plate technique, advantage is taken of the fact that a stiff, free-free metal plate can exhibit very high frequency resonances. The article to be tested is mounted to an aluminum or steel plate, and the plate is subsequently suspended in mid-air. A metal pendulum is then swung into contact with the dale. inducing transient vibration. If' the frequency response of the mounted test article is measured with an accelerometer, a plot such as that illustrated in Figu re 4 can result.

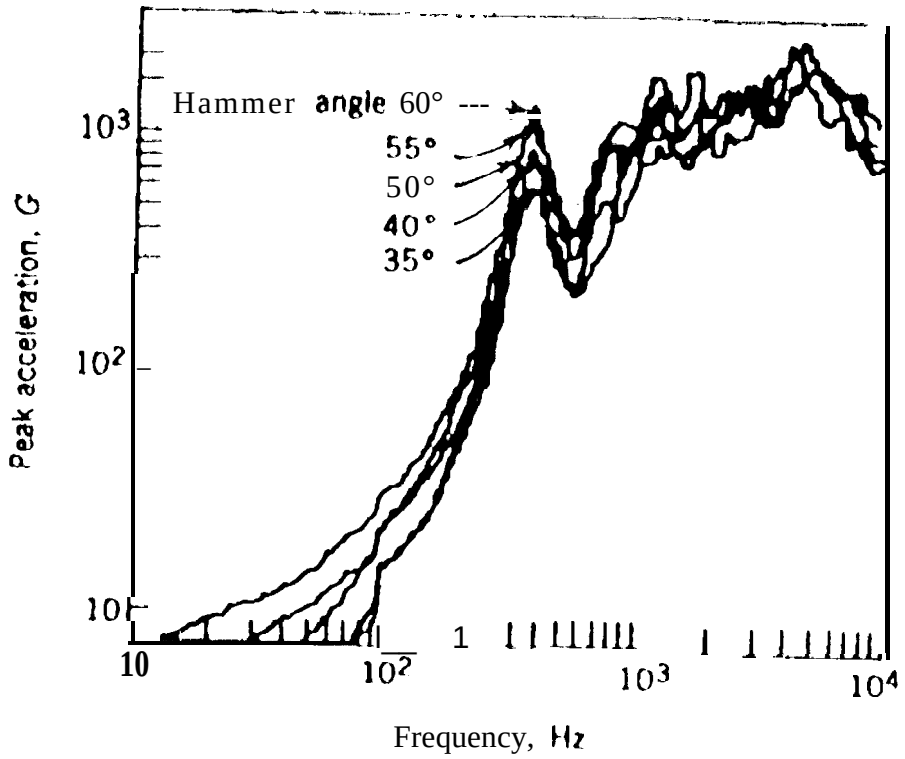
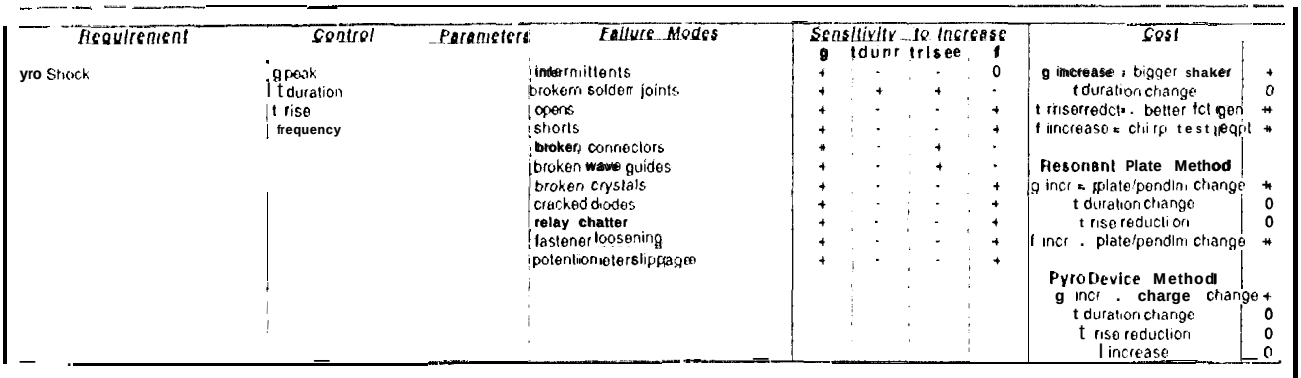



Figure 4 - Response Spectrum in **Resonant** l'late **Test**

Although this technique can clearly produce a response exhibiting the desired trend of increasing, acceleration with increasing freq uency, it is still less than ideal. Tuning of the response spectrum such that the correct accelerations occur at the desired frequencies is very difficult, involving modification of the plate thickness, shape or suspension method, modification of similar hammer characteristics, or mollification of the hammer swing angle as illustrated in Figure 4. These activit ics arc time consumi ng and generall y based on trial and error, and may never produce the correct response spectrum.

The best pyrotechnic shock test method, then, is one which utilizes pyrotechnic devices. Due to safe.ty, facility and related requirements, this can be an expensive proposition. However, considering the time which might otherwise. be wasted during the construct of a simulation, and considering, the potential for overdesign or underdesign of hardware which could occur if the simulation is inaccurate, the pyro method may in fact be a bargain. It should be utilized if at all possible.

Armed With our vast knowledge of the primary shock testing methods, WC can now present appropriate test control parameters, the sensitivity Of failure modes to changes in these parameters, and cost tradeoffs associated with each. Figure S provide.s a summary matrix of this in formation.



| Requirement | Control Parameters | Failure Modes | Sensitivity to Increase g | t duration | t rise | f | Cost | |
|---|---|---|---|---|---|---|---|---|
| yro Shock | g peak | intermittents | + | - | - | 0 | g increase = bigger shaker | + |
| | t duration | broken solder joints | + | + | + | - | t duration change | 0 |
| | t rise | opens | + | - | - | + | t rise reduction = better fidelity | + |
| | frequency | shorts | + | - | - | + | f increase = chirp test required | + |
| | | broken connectors | + | - | + | - | | |
| | | broken wave guides | + | - | + | - | Resonant Plate Method | |
| | | broken crystals | + | - | - | + | g incr = plate/pendlm change | + |
| | | cracked diodes | + | - | - | + | t duration change | 0 |
| | | relay chatter | + | - | - | + | t rise reduction | 0 |
| | | fastener loosening | + | - | - | + | f incr = plate/pendlm change | + |
| | | potentiometer slippage | + | - | - | + | | |
| | | | | | | | Pyro Device Method | |
| | | | | | | | g incr = charge change | + |
| | | | | | | | t duration change | 0 |
| | | | | | | | t rise reduction | 0 |
| | | | | | | | f increase | 0 |

**Figure** S - Control Parameter Sensitivity and **Cost** Sensitivity

## 4.0 References


1. Moening, C. J., "Pyrotechnic Shock Flight Failures," The Aerospace Corporation, 1984.


## 5.0 Bibliography


1. Steinberg, D. S., Vibration Analysis for Electronic Equipment, New York: John Wiley & sons, 1986.
2. Markstein, Howard W., "Designing Electronics for High Vibration and Shock," Electronic Packaging & Production, April 1987, pp. 40-43.

# 3. Radiation Design Margin Requirement

## 1.0 Objectives

One of the design drivers of spacecraft is the requirement to survive in the radiation environment expected to be encountered throughout the mission. Flight assemblies shall be designed to withstand ionization effects and displacement damage resulting from the flight radiation environment with the required radiation design margin (RDM).

The definition of RDM is the ratio of radiation capability of the part or component for a given application to the expected radiation environment at their respective location during the mission. The part/component radiation capability is defined to be the fluence (or dose), flux (or dose rate) of charged particles or nuclear radiation which will produce enough change (degradation or radiation-induced interference) in the part characteristics to cause the part to operate out side of its specification for the particular circuit application.

The RDM requirement is imposed on assemblies or subsystems to assure reliable operation and to minimize risk, especially in mission critical applications. The general use of an RDM acknowledges the uncertainties in environmental calculations and part radiation hardness determinations,

## 2.0 Typical Requirements

Based on flight experiences, it is standard practice at JPL to require an RDM of 2 for most applications if only the inadvertent shielding of the surrounding, spacecraft or instrument enclosure materials are considered in the radiation/shielding analysis. However it requires an RDM of 3 when local shielding, such as component/part package or spot shielding, is taken into account.

The RDM requirement does not apply to single event effects (SEE), such as single event upset (SEU), single event latchup (SEL), etc., since SEE is evaluated on a probabilistic basis.

## 2.1 Rationale

The uncertainties in radiation environment estimates and the part or component radiation capability determinations lead to RDM values between 3.5 to 11.5 (Ref. 1). Historically, the introduction of an RDM of 2 stems from the Voyager Project and was established based solely on not having sufficient mass allowance for shielding. An RDM much greater than 2, perhaps as high as 10, would have been selected to cover all uncertainties if there had been sufficient mass available (Ref. 1).

An RDM of 3 is imposed when local shielding, such as component/part package or spot shielding, is taken into account, There is an implied greater risk associated with taking the local shielding into consideration because this is done in cases where soft parts, rather than inherently hard parts, must be used that are dependent on local shielding and their calculated shielding effectiveness.

### 2.1.1 Failure Modes

#### (1) Long-Term ionization Effects

Potential problems with the electronics and material arise from the long-term effects of ionizing radiation. The magnitude of long-term ionization is a function primarily of ionizing energy deposition, i.e.. the dose measured in rads in the material in question.

In semiconductor devices, these are manifested 'in charges being trapped in insulating layers on the surface of the semiconductor devices. They are most important in MOS structures in which trapped charges in the gate oxide layer produce a change in the apparent gate volt age. Trapped charges in surface passivation layers are also important in junction devices where they may produce an inversion layer that spreads out over the effective surface area, thereby increasing the recombination-generation currents. '1 'hese currents are most import ant in bipolar t ransistors that arc operated at low collector currents and in n-channel JFET devices. The susceptibilit y to surface recombination depends on the quality Of the oxide layer and the applied electric field.

In optical materials, long-term ionization effects appear primarily as an increase in optical absorption. These arc usuall y manifestat ion of charges trapping at a prc-existing defect, so the absorption rate is a strong function of the initial mate.rial properties. For example, fused quartz generally colors less than alkali glasses for a given ionizing dose.

In quartz crystal used for precision oscillators or filters, long-term ionization effects can produce significant resonant-frequency shifts. Again the.rc is a strong, dependence upon the type of material used. Natural quartz shows the largest frequency shift for a given ionizing dose, synthetic quartz shows less, and swept synthetic quartz shows even less. in these cases proper selection of the quartz crystal growth method can minimize the. effect.

The devices and materials of concern and the most serious radiation induced effects are:

(1) h40S devices (threshold voltage shift, enhanced leakage).

(2) Bipolar transistors ($h_{FE}$ degradation, especially at low $I_C$ ; leakage current), and junction field effects transistors (JFETs) (enhanced source-drain leakage current).

(3) Analog microcircuits (offset voltage, offset current and bias-current changes, gain degradat ion).

(4) Digital microcircuits (enhanced transistor leakage, or logic failure due to ionizing close induced $h_{FE}$ & $V_T$ changes).

**(5)** Quartz resonant crystals (frequency shifts).

(6) Optical mate.rials (increased absorption).

(7) External polymeric surfaces (mechanical degradat ion).

**(2) Transient** ionization **Effects (Interference)**

Interference is defined as transient ionization effects that persist only while the electronics arc being irradiated, and whose severity is generally proportional to the dose rate. Interference effects depend primarily cm the rate of ionization energy deposition, i.e., the dose rate measured in rad/s.

'1'here. are four t ypcs of interference in electronics devices and optical materials:

(1) Primary photocurrents in low current sensitive input stages to the electronics.

(2) Electron emission from cathodes of electron multiplier-type detectors.

(3) Ionization-induced conductivity in photo-sensitive materials, such as those in detector surfaces,

(4) Ionization-induced fluorescence in optical materials, such as detector windows and lenses (fluorescence efficiencies vary strongly with the types of material).

### (3) Displacement Effects

1 Displacement of atoms in crystal lattices cause permanent changes to material properties. The expected proton and electron fluences usual 1 y do not represent as severe an environment fOr displacement effects as for long-term ionization effects. Therefore, only the most sensitive devices will be affected significantly by displacement effects.

I Displacement effects can affect the following devices and properties in the electronics:

(]) Bipolar transistors with low $f_1$ ($h_{FE}$, $V_{CE\ SAT}$, $V_{BE\ SAT}$).

(2) PN junction diodes ($V_F$, $V_B$).

(3) Light emitting diodes (LED) ($V_F$, $V_B$, light emitting efficiency).

(4) semiconductor photodetectors (quantum efficiency).

(5) Devices incorporating lateral p-n-p transistors ($h_{FI}$, $V_{CE\ SAT}$, $V_{BE\ SAT}$).

(6) MOSFETs (resistance, leakage current).

## 2.1.2 Supporting Data

The JPL PFR database was searched for types of failures and failure modes recorded during the. radiat ion tests and in flight. An abstract of some of the 1'1 'R data related to radiat ion c. ffects arc shown in Table 1.

Table ]. JPL Radiation Effects Problem/Failure Histor

| S/C | PFR # | Environment | Description | Fai | Failure Mode |
|---|---|---|---|---|---|
| Voyager | 41048 | Flight | No counts in fate channels of HET 2 telescope | Its the | Probably one of the 3 hi-polar transistors in the circuit failed due to radiation |
| Galileo | 52602 | Flight | Observed noise spikes characteristic of radiation induced events in SS1 | A l | A likely correlation with high solar activity level |
| Galileo | 41341 | Test | The ultra stable oscillator (USO) shifted frequency 1.676 Hz due to a 5 Krads dose | (2) LM res | (1) negative frequency shift is to be expected when swept synthetic quartz is irradiated<br>(2) the offset voltage changes in the LM108HR of the inner oven control circuit resulting from radiation |
| Galileo | 44287 | Test | Some of CDS's memory SRAMs got worse with radiation | thr | Significant degradation of the read disturb threshold |

## 3.0 Tradeoffs

Often an RDM of 2 is perceived by many people as being overl y conservative. The selection of an RDM may be somewhat arbitrary and will tend to be driven by mass limitations, acceptable risk versus cost, and the total radiation hardness program.

Projects typically have resources and mass limitations which preclude usage of more conservative RDMs. Based on the "best" radiation model at the time, the. part radiation hardness test data, and the expected mass and other resource limitations, a radiation design factor of 2 (3 if local shield is

considered) is required for spacecraft flight elements. The term used to describe this radiation design factor is "radiation design margin", and this is the source of most common misunderstanding. The problem arises from the fact that there are significant uncertainties in all the elements in the radiation susceptibility calculations, and the term "radiation design margin" implies a known factor of safety, which in turn implies a large degree of certainty of survival in the radiation environment. For this reason RDM which implies a margin is really a misnomer. It may be more appropriate to refer to a radiation design factor and not inadvertently mislead people to believe a conservative margin exists. An RDM of 2 is not, nor was it ever, intended to imply 100% margin as it has sometimes been misconstrued to mean. An RDM of 2 does not cover the uncertainties as indicated in Reference 1. However, in the world of practicality an RDM of 2 was all that was affordable on Voyager, and it worked on the one spacecraft that was tested. It is important to reiterate that there are uncertainties in environmental calculations and part radiation hardness determinations in the use of RDM.

### (1) Radiation Hardness Determination

There are at least four quantities that can contribute to the uncertainty in the part radiation capability: the part type, the manufacturing process, the circuit design, and the particular circuit application. There are many different part types, many circuit designs and applications and perhaps several different manufacturing processes, Consequently, the uncertainty in the part capability has to be sufficiently large to account for the large variations from part to part. Most of these are difficult to quantify and testing is the only method of determining the radiation capability to be expected in a given flight lot. Even though the uncertainty for any one specific part may be quite small, different radiation test conditions can generate different capability values, For some linear integrated circuit devices, the total ionizing close ('1'111) capability could drop dramatically if tested with low dose rate instead of high close rate. For example, OP42 was rated a radiation-hard device (> 100 Krads) in the past but was recently found to be very soft (~ 15 Krads or lower) when tested with low dose rate which better simulated the flight environment,

As electronics parts now have higher capacity and smaller volume compared to those used on Voyager and other spacecraft, it is prudent to carefully re-examine RDMs of higher magnitude on future spacecraft programs or to refine the part radiation hardness determination technique if an RDM of 2 or lower is demanded. The part radiation hardness test is generally a cost driver. This is primarily due to the fact that a more accurate test requires more samples, more realistic flight simulating radiation sources and conditions, and longer test time.

The alternative to overcoming the test uncertainties is to perform the worst case analysis (WCA) for the circuit applications. For example, if a bipolar transistor was rated 50 Krads in term of $h_{FE}$ degradation, but the parameters shift due to an irradiation of 100 Krads is still acceptable based on the worst case analysis, this part has the required RDM of 2 if the local environment is 50 Krads.

### (2) Radiation Environment Calculation

The local ambient radiation environment is dependent on the mission design, the environmental radiation models, the radiation transport code, and the spacecraft mass mock]. The calculated radiation environment might be the total ionizing does (TID), 20 MeV equivalent proton fluence for displacement damage, or flux for detector interference effects.

The uncertainty in the radiation model depends on the environment in question and the mission design. Uncertainties in the mission design are difficult to quantify. The parameters involved here. include the trajectory (heliocentric distance, mission length, altitude, inclination, etc. ) and launch date. The uncertainty in the radiation environment depends on the environment in question. As an example, prediction of proton fluences from solar flares is treated probabilistically and the discrepancy between predictions for the 10 MeV fluence between two different solar flare models

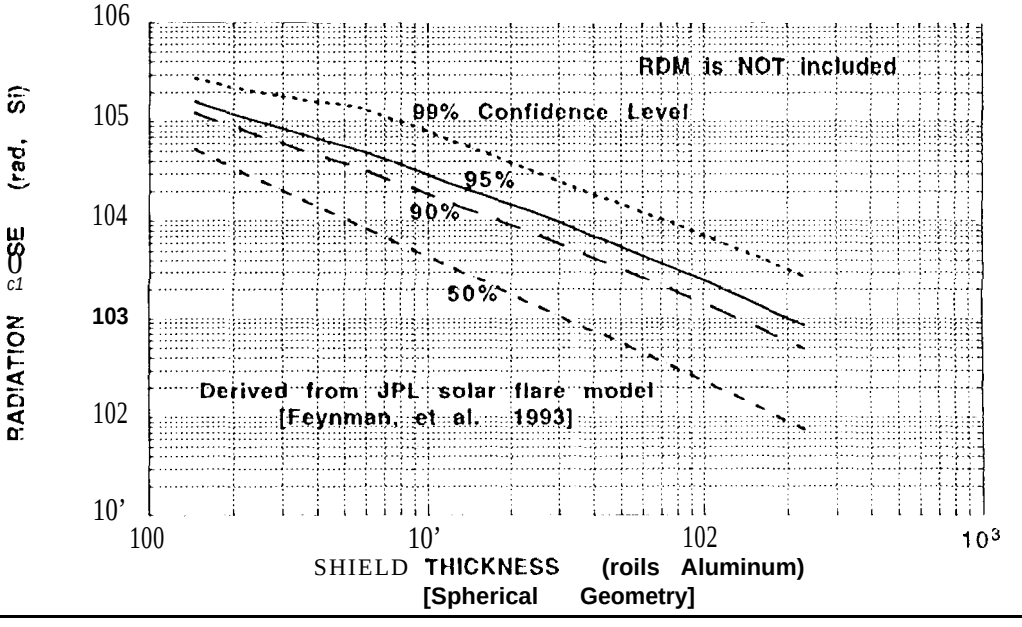
is a factor of 2 (at the 95% confidence level) (Ref. 1). Similarly, the uncertainties in the Jovian trapped electron environment and the Earth's trapped radiation proton model AP8 are also estimated to be a factor of 2. The uncertainties resulting from the use of different radiation transport codes and different spacecraft mass models are generally less than a factor of 2 (Ref. 1).

Typically, once the mission design is confirmed, the TID as a function of shielding thickness (dose-depth data) are generated for a simplified geometric mass model, such as the spherical shell model. Figure 1 is an example of a flight mission at 1 AU from the sun during the solar max period. It is standard practice to apply the dose-depth curve at 95% confidence level for the flight assembly (unit) design. This radiation dose curve can be used to obtain conservative "first-look" shielded dose values without hardware configuration modeling. These dose plots should only be used to obtain dose value by using the minimum shield thickness applicable to a given hardware location. Since these plots do not represent flight hardware configurations, they should be used for design assessment only if they are applied in a conservative manner (minimum shield thickness used). If the concerned part does not meet the RDM of 2 requirement based on this conservative TID level, a three dimensional mass model simulating the fright assembly (unit) is then constructed for the radiation transport code. The resulting TID level will be lower than the TID data from the spherical shell model and therefore the concerned part is more likely to meet the RDM requirement. However, when the part/component package has to be included in the 3D mass model or a spot shit.]~i has to be added, the RDM is increased from 2 to 3 as explained earlier. The more extensive radiation/shielding calculations tend to be a cost driver, but it relieves the shielding requirement and therefore saves more mass.

Radiation/shielding analysis is relatively cheap compared to spot shielding design/implementation or part radiation hardness tests. It takes several days to analyze TID with a simplified mass model, such as a box, or several weeks to generate more accurate TID results with a more realistic mass model to simulate the flight assembly (unit). The resulting lower TID level reduces the unnecessary shielding mass and relieves the part hardness test rigidity.

Figure 1

RADIATION DOSE from SOLAR FLARE PROTONS
for 1 year at 1AU



Failure mode sensitivities and cost tradeoffs for the radiation design margin (RDM) requirement are illustrated in Table 2.

Table 2. Control Parameter Sensitivity and Cost Sensitivity

| Requirement | Control Parameter | Failure Modes | Sensitivity to Increas Failures | | Cost | |
|---|---|---|---|---|---|---|
| | | | P | D | | |
| Radiation Design Margin (RDM = P/D) | Radiation Capability (P) | Long-Term Ionization Effects | | + | Refining Radiation Capability Test | + |
| | Local Radiation Environment (D) | Transient Ionization Effects | | + | Refining Radiation Environment Calculation | + |
| | | Displacement Effects | | + | | |

## 4.0 References

1. JPL IOM 5217-88-39, "Radiation Design Margins", S. B. Gabriel to Distribution, September 22, 1988.

# 4. Minimum Operating Time Requirement

## 1.0 Objectives

The objectives of operating assemblies or subsystems for a minimum period of time or number of cycles are to verify their operation in accordance with the design requirements and to ensure that the manufacturing workmanship or integration processes have not compromised their reliability. It also verifies the appropriateness of the design for the mission, based on the anticipated failure modes.

## 2.0 Typical Requirements

Operational hours (for electronics) or the number of mechanical cycles (for periodic or continuous cycling, mechanical units) should be sufficient to demonstrate operation despite of design, workmanship or integration problems.

Minimum operating time requirements, as specified in JPL-D-8966, for different spacecraft classes are:

1,000 hours for Class A spacecraft
500 hours for Class B spacecraft
200 hours for Classes C and D spacecraft
Mechanical cycling is 1.5 times the mission-required cycles

Industry requirements for electronic burn-in vary from 100 to 2,000 hours. in most cases, the available specifications for operational hour/cycle requirements do not provide the rationale or methodology for their determination.

### 2.1 Rationale

The operational duration and power cycling of electronics, or the number of cycles of mechanical cycling devices serve to uncover electrical/mechanical infant mortality or latent defects, thus assuring spacecraft reliability. They also provide. information on integrity, as well as operational or reliability expectancy of the equipment being tested, During the testing, some or all of the expected stresses are applied to the equipment. Depending on the failure modes expected for the applied stresses and their duration, failures of weak components or assemblies will appear on a certain time scale. As indicated in Reference 1, time dependent failure mechanisms can be important for a significant number of hardware elements.

#### 2,1.1 Failure Modes

Examples of time-dependent deficiencies and defects are summarized below:

1. Design deficiencies, such as:

   a. Electrical or mechanical component, or mechanical assembly wearout caused by excessive stresses, poor tolerancing, or workmanship.
   b. Electrical or mechanical over-stress of components causing hard failures.
   c. Thermal design deficiency causing component parametric drift and an increase in inherent failure rate.
   d. Loss or inadequate lubrication of mechanical cycling devices.

2. Workmanship defects, such as:

a. Poor solder joints (also tcIllJJcratLlrc/cycle dependence).
b. Damaged component hermetic encapsulation.
c. Inadequate welding of pyro-activated devices (such as bellows) causing leaks and failure to actuate.

3. Software problems, such as:

a, 1 Errors that can only be identified when the codes in question arc executed. This may take a long period of time.

The JPL Problem Failure Reporting, PI 'R, database was searched for failure modes found in tests and the test operat ional time and/or operational cycle duration. Examples of some of the failure modes arc tabulated below:

**Examples of Failure Modes**

| Design (electrical) | Design (mechanical) | Workmanship |
|---|---|---|
| Functional anomalies<br>Out of spcc operation<br>Detectable over-stress<br>Electronic instabilities<br>Parameter variation<br>Sneak circuits<br>Shorting to ground<br>Open circuits<br>Inadequate interfaces<br>Cracked PCB traces | Poor solder joints<br>Overheating<br>Material interference (dissimilar materials) | Poor solder joints<br>1 ow or high torque on fasteners<br>Cracks in component encapsulat ion |

1 Each failure mode typically has a different time dependency that requires individual consideration. I For some failure modes, "operational duration/cycle requirements 'may be statistical y estimated from a know] edge of the detailed mechanisms of specific failure modes. I For other time- or cycle-sensit ive failure modes, they may be determined through fact orial design or estimated from a database search. For many of the failure modes, the minimum operating time based on this factorial design has been determined and they can be found in the. literature.

### 2.1.2 Supporting Data and Recommendations

The J]']. PFR database was searched to determine the t ypcs of failures and failure modes rccordcd during operational time or cycling duration tests. An abstract of some of the PFR data is shown in "1'able I.

The JPL flight anomalies database was examined to establish their time. or cycle dependence. For the latter, some orbiter S/C data from GSFC were also reviewed, together with the J}']. interplanetary S/C database. The reason for including both orbiters and interplanetary S/C is that the. New Millennium is a series of S/C which will be designed and manufactured more like commercial orbiters than traditional JPL interplanetary S/C. I Data from some orbiters show flight failures that arc direct] y related to the operating time or operational cycle duration, possibly indicating an inadequacy of testing.

Table ]. Ground Test Anomalies Related to Operational Time ant]/or Cycling for Interplanetary and Orbiter S/C.

| S/C | PFR # | Description | Nature of Test | comment |
|---|---|---|---|---|
| Viking | 30716 | Power events meter for TMU-a failed cycling | Power Cycling | l'owe] monitor drawer problem |
| Voyager | 36144 | Scope. display not calibrated at screen top | Operating Time | Found defective oscilloscope |
| Voyager | 37221 | Chain A #03 signals incorrect frequency width | S/W 1 'rr or | Shown when this Code executed |
| Voyager | 40330 | Erratic limit cycling in pm burn mode | S/W } 'rror | Shown when this Code executed |
| Voyager | 40724 | Shunt radiator simulator relay cycling | Cycling | |
| Voyager | 1055S'1 | Prop valve leaked after hot cycling | Cycling | |
| **Acoustic** | **40529** | **1,&R sample handler** retraction time increased | Operating **time or cycling** | Wearout, mechanical |
| ATMOS | 31744 | No flight vib. isolator helicoil lock **capability** | Operating time | Wearout, fasteners |
| ATMOS | 51054 | IR detector could not be cooled down to its normal temp. | Operating time | |
| BETSCE | **Z10249** | **Valve** switch drive circuit failure | Power Switching on/of f | |
| Cassini | 59729 | S/W error in hot and cold temperature | Execution time | S/W errors should not be dependent on temperature |
| Galileo | 54308 | Lcet air conditioning failed/CDS-SE overheated | Operating time | |
| Galileo | 54570 | PPE failed to achieve 1.5 ppm dewpoint spec. | Operating time | New filters installed |
| Galileo | 41308 | S-hand command switch sticks in S/C HI position | Operating Time | Switch wearout |
| Microwave Limb Sounder | 58099 | The antenna is not forward stepping | Operating Time/Cycling | Wearout; Flight Failure. Motor bearings |
| NASA Scatterometer | z1o100 | Configuration: dss b, TWTA #2 selected; receive-only mode | Power cycling | |
| Pioneer | 100723 | Preamp output low on turn-on, increases as a function of the operating time. (contamination found | Operating time | Would not be found without test. |
| SIR-C | 56172 | Cassette tape loading problem led to power supply failure. Cycling power on/off caused the PS failure | Power cycling | |
| Tiros | 1316 | Gunn oscillator SW regulator PWR Supply failed | Operating time | 15V shorted to the ground |
| WFPC | 49460 | A latch plate damaged by collar on the shaft | Operating time | Reworked; Galled surface machined, base cleaned, surface re-lubed. |

No definitive conclusions could be made about the appropriate test or cycling duration from the present JPL PFR Database, as the test time. for the failures is not routinely recorded. With cooperation from projects, efforts are underway to ensure this information is always entered in the d at abase.

The operational time into flight can be obtained from the flight data. But, these data do not assure knowledge of how long a particular assembly (unit) has been powered on or the number of cycles accumulated on a particular switch since. they do not include ground test information. However, this information can be obtained from ground testing records or from test personnel. Table 1 I shows examples of flight anomalies relate.ci to the operating, time or cycling of orbiters and an interplanetary S/C (Voyager).

Table II. Examples of Flight Anomalies Related to the Operating Time or Cycling of Orbiters and an Interplanetary S/C (Voyager).

| PFR No. | S/C | Sub-system | Assem. Part | Symptom | Cause | Action | Recommendations | Trs o a'l |
|---|---|---|---|---|---|---|---|---|
| A01282 | COBE | Structural | Solar Array W-BOP | Wing-B outer panel telemetry displays > 95% deployment Should show lock position as nominal. (switch did become functional after a period of about 6 months.) Comment: no effect on COBE mission. | Microswitch did not fully close (make contact). 1 he microswitch TLM suddenly indicated a "lock" condition. | None possible - potentiometer telemetry shows deployment to be 100% | Always provide backup device to microswitch. | ( |
| 101059 | AP | Gamma Ray Spectro-meter | Elec-tronics | Gain shift occurred in lunar orbit/sci data ok. | Other causes | Traced to aging characteristic of sensor. Pre-aged sensors w/simulated space environment. | Age AGRS S/N 003 (flight spare unit) in same manner as S/N 004 (Apollo 16 flight unit). Verify GRS calibration validity of each flight unit subsequent to aging. | 7 |
| A00369 | DE | Fine Sun Sensor | | Sun sensor beta angle electronics changed gain and bias settings for no known reason. | Actual cause unknown Suspect degradation of LM108 in processing electronics of one of four fine bit channels. | Beta readout continues to degrade with time. Use alpha inform nation only in producing attitude information. Definite attitude not affected. | | 45 |
| 897 | ERBS | Sun Sensors | Harness (FRM SS2) | Incorrect alpha angles from sun sensor #2. Eight lsb telemetry bits are inverted. The ninth bit is incorrect. | Spacecraft sun sensor #2 was wired incorrectly. (That is, harness from sun sensor #2 to tile electronics box was mis-wired two wires reversed). | Flight dynamics (code 581) changed their ground calibrations to fully correct for this error in the spacecraft. | Flight dynamics (cede 581 ) changed their ground calibrations to fully correct for this error in the spacecraft. Action to be taken on follow-up: none. | 7 |
| 11031 | Voyager | RF Sub system | | S-band HGA drive dropped 5 dn analysis of trend data, indicating antenna drive had been decreasing and becoming increasingly noisy since day 289 (1977). This confirmed problem in the S-band SSA in S/C 32. | High thermal delta of the transistor - MSC 3005. Detailed defect of the transistor remained unknown - probably wearout phenomena | None. | None - used as it was. Comments: for futur flights the MSC 3005 should be replaced with transistors having barrier metal and go through an extended burn-in. Performance was normal in the low power mode on both amplifiers. | 189 |

From this table. it is apparent that some design failures (wearout is considered as a design failure in this discussion) during flight could have been prevented by appropriate testing 'and design improvement. Test acceleration may be a feasible solution to mitigate flight failures occurring, late in flight for long missions.

### 2.1.3 Calculation of Total Minimum Operating Time

The minimum operating time is determined based on the Duane graphical reliability growth model that has been used in industry for over a decade. The relationship between the initial and final mean time between failures (MTBF's) is given below:

$$\frac{\theta_F}{\theta_0} = \frac{1}{1-\alpha} \cdot \frac{t_F}{t_0}^{\alpha}$$

where:

$\theta_F$ = achieved final MTBF
$\theta_0$ = initial MTBF
$t_F$ = operational test duration
to= initial test time (short burn-in time to correct for workmanship flaws)
$\alpha$ = growth rate

During operational testing, a S/C is considered a repairable system, thus the reciprocal of its final MTBF is its failure rate at the beginning of flight. Since the initial and final MTBF vary exponentially with the growth rate, small variations in the growth rate result in significant changes in the achieved final MTBF or the operational test time duration.

Test durations, shown in Table 111, arc calculated with the following assumptions:

1. The subsystems or a combination of them have been functionally tested prior to S/C integration.
2. All test times are additive.
3. 'l'he design and construction of interplanetary S/C arc similar to Earth orbiters.
4. The test failure correction uses an aggressive, industry-recommended average reliability growth rate of $\alpha = 0.6$. For further cost savings, a more aggressive failure investigation and correction process may be introduced to achieve. a higher reliability growth rate of $\alpha = 0.65$.
5. Test failure modes include design, workmanship, and random failures.
6. Scored test failures are critical at the subsystem level and one failure is fatal. All failures are assumed independent. However, in the case of critical, dependent/induced failures, only the first, original failure is scored.
7. The failure rate at launch is assumed to be 10 times the desired mission failure rate, as per widely-accepted industry rule for newly-developed or new] y-prod uced items.
8. Mission duration dots not have any influence on test duration. The S/C arc designed and constructed as per mission duration requirements.

Table 111. Operational Test Duration, Calculated for Average Reliability Growth Rates of $\alpha = 0.6$ (currently attainable with existing JPL failure investigation and concurrent engineering practices) and $\alpha = 0.65$ (Recommended for Faster Better Cheaper Missions).

| Item | Failure Type | Calculated Test Duration, $\alpha = 0.6$ (hours) | Calculated Test Duration, $\alpha = 0.65$ (hours) |
|---|---|---|---|
| Subsystems, a group of subsystems, or a single string S/C. | Design<br>Workmanship<br>Random (see Note 1) | 500<br>(see Note 2) | 350<br>(see Note 2) |
| Integrated system (assumed integration completed after subsystem testing. | Workmanship<br>Design | 2?00<br>(see Note 3) | 170<br>(see Note 3) |
| Total Test Time | Worst case | 700<br>(see Note 4) | 520<br>(see Note 4) |
| | Normal | 500<br>(see Note 5) | 350<br>(see Note 6) |

Note. 1. Reduced random failures assume system improvement (i. c.. a better quality or higher rated component, design improvement, fault protection, etc.). Replacement of the failed component does not guarantee elimination of a future failure of the same component.

Note 2. Test' times can be accumulated during various engineering evaluation or environmental tests.

Note 3. Additional test times at the integrated system level arc needed to screen for workmanship or design (compatibility) defects that may be introduced during integration or as a result of subsystem interaction.

Note 4. This is a case in which all tests are conducted sequentially.

Note 5. Normally, 300 hours at the. subsystem level and 200 hours at the integrated system level, giving the require.d total of 500 hours.

Note 6. Normally, 180 hours at the subsystem level and 170 hours at the integrated system level, giving the required total of 350 hours.

The number of test cycles of mechanical devices depends on whether they have previously been t ested. Mechanical devices, in most cases, are. also subject to normal wearout. Therefore, the number of test cycles depends on the desired mission reliability. If the average number of wearout desired is 4 (normally the case with mechanical cycling devices), then the number of test cycles should be 1.7 times the required mission cycles. However, for Faster Better Cheaper Missions it is recommended that 1.5 times the required mission cycles be used, resulting in an increased average number of wearout of between 5 and 6.

Software operation cannot be separated easil y from the hardware's and its reliability must also be taken in considerat ion. '] 'he software should be tested with a test compressi on" factor and its reliabil it y determined with a test durat ion determined based on the required or desired reliabilit y.

## 3.0 Tradeoffs

System operation time is both a cost and schedule driver. Operation time may be reduced to prolong the useful life of devices that are subject to wearout, if cycling t ime has been accumulated. At JPL, the minimum operating time for an integrated system may be reduced if operating, times have been accumulated on individual assemblies. operating times at the assembly (unit) level may be sufficient to disclose failure modes, such as poor solder joints, out of spec operation, parameter variation, materials interference, PCB defects, etc. The accumulated test t imes on assemblies under

various test conditions (environmental or engineering evaluations) can considerably reduce the minimum operating time required for the integrated S/C syst cm, and stil 1 provide reasonable verification of S/C integrity, robustness, and expected mission reliability.

Failure mode sensitivities and cost tradeoffs for the minimum operating time and minimum operat i ng c ycles requirements arc illustrated in l'able. 1 V. During minimum t ime operat ion it is also important to exercise all potential combinations of operating modes of the hardware at least once to identify mission critical modes.

Table IV. Control Parameter Sensitivity and Cost Sensitivity.

| Require-ment | Control Parameters | Failure Mode.s | Sensitivity to Increased Failures | | | | cost | |
|---|---|---|---|---|---|---|---|---|
| | | | dur | ES | TS | MS | | |
| -qRiiii--Time | 1 Duration | Funct. anomaly | + | + | + | 0 | Duration | + |
| | I Electrical stress (ES) | Out of spec. operation | + | 4 | + | 0 | Electrical stress | + |
| | '1 'henna] stress (TS) | Elect-wear | + | + | + | 0 | Thermal stress | + |
| | Mechanical stress (MS) | Shorts | + | + | 0 | + | Mechanical stress | + |
| | | Poor solder joints | + | + | + | -1 | | |
| | | Parameter variation | +- | + | + | 0 | | |
| | | Open circuits | + | i- | -t | + | | |
| | | Cracks | + | 0 | + | + | | |
| | | Poor bonding | -t | -1 | -t | -1 | | |
| | | Poor interfaces | + | + - | () | + | | |
| | | Cracked CB traces | '-t | o | + | -t | | |
| | | | | | | | | |
| Operating Cycles | Duration | Braking | + | 0 | 0 | + | Duration | + |
| | Electrical stress (ES) | Deformation | + | 0 | + | + | Electrical stress | + + |
| | Thermal stress ("1'S) | Elect-wear | + | 0 | + | + | Thermal stress | + |
| | Mechanical stress (MS) | Shorts | + | + | + | + | Mechanical stress | + |
| | | Poor solder joints | + | + | + | + | | |
| | | Parameter variation | + | 0 | + | 0 | | |
| | | Open circuits | + | + | + | + | | |
| | | Cracks | + | 0 | + | + | | |
| | | Poor bonding | + | + | + | + | | |
| | | Poor interfaces | + | + | + | + | | |

## 4.0 References

1. MIL-STD-1450C, Test Requirements for Launch, Upper-Stage, and Space Vehicles.

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1. MIL-STD-810E, Environmental Test Methods.
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# 5. System Level Fault Tree

## 1.0 objectives

The System Level Fault Tree (SFT) pictorially depicts those failure modes that result in mission failure. In addition, the SFT identifies single point failures (SPFs) and depicts mitigating design features that are implemented. The SFT analyzes and documents the significant high-level system functional failure modes that are important to various phases of the mission. The SFT provides a seamless link between the system level functional failure modes and the failure modes identified in the subsystem Failure Modes, Effects and Criticality Analyses (FMECAs).

## 2.0 Typical **Requirements**

Develop a spacecraft level fault tree for each of the mission phases (i.e., launch, cruise, orbit insertion, tour, etc.). Depict the spacecraft and ground system functional failure modes for those phases. Guidelines for performing Fault Tree Analysis (FTA) arc. provided in J}'l. D-5703 (Ref. 1). The SFT is supported by the subsystem level FMECAs.

### 2.1 Rationale

The SFT approach provides a systematic, logic based, graphical approach to analyze and document the major failure modes that can lead to loss of the mission, The SFT displays the logical relationship between the system level failure modes anti the lower level events that lead to these failure modes. This representation provides the development team, from the manager to the working level engineer, with a view of significant threats to the mission. It also offers the team and its re.view board a chance to add failure modes not yet included in the model. This improves the chancre of including a complete set of failure modes. The guidelines in JPL D-5703 are provided to promote uniformity of analysis methods within and across various projects. This approach is beneficial for both the preparer and the. independent reviewer,

#### 2.1.1 Relevant **Failure Modes**

The SFT can be used to represent all possible failure mode, but its presence or absence does not avoid or cause any one specific failure mode. The SF"]' is, however, especially useful in identifying interface problems between two or more hardware elements when one clement has a failure and another is required to perform some function to mitigate the effects of the failure, For example, consider a design where there is no autonomous fault protection that deals with a particular failure. in this case the plan is to have ground support respond to the failure with some mitigating action. If the required response time is significantly shorter than the. mission two-way light time, the ground system action would be of no use. This type of situation could, and has been found and corrected.

### 2.2 Methods

The SFT should be developed in the early design phases, and progressively refined and updated as the. design evolves. The initial SFT will generally represent high level functional blocks (c. g., units, equipment, etc. ), but later become more definitive at lower levels as the design matures. The first step in developing the SFT is to develop Functional Flow Diagrams (FFD) depicting all the functions required to achieve the mission objective. The FFD depicts all the ways the top level function is achieved. For example, if there is block or functional redundancy within the spacecraft the alternate paths for providing the function are depicted. Once the FFD is completed, the SFT can be developed. in the SFT, the top level functional failure is indicated as well as all the lower level events that can lead to the top level failure. Some failure modes require onl y one. of several

events to lead to the upper level failure. in this case, the lower level failure would be depicted as inputs to an "or" gate under the upper level failure, thus indicating that any one of these events would lead to the upper level failure. Other failure modes require two or more events to lead to the upper level failure. In this case the lower level events would be depicted as inputs to an "and" gate under the upper failure, thus indicating that ail of the events under the "anti" gate are required for the upper level failure to occur. As is done in the FFD, block or functional redundancy is depicted in the SFT. in most cases, various phases of the mission require slightly different lower level functions, so each phase may have a distinct SFT. These can be considered as subtrees of the overall mission SFT. Guidelines for performing FTA arc provided in JPL D-5703 (Ref. 1).

## 3.0 Tradeoffs

The project tradeoff for doing the SFT is based on the actual cost of developing the SFT model versus the reduction in expected cost (in a probabilistic sense) associated with an unidentified inflight failure occurring. Specifically, the actual cost includes: developing the functional flow diagrams, the SFT models and the associated design interface support. These actual costs arc compared to the reduction in expected cost of an inflight failure. The latter cost is based on several factors including: the reduction in the probability of an inflight failure associated with an unidentified failure mode., the fraction of the mission lost and the monetary value of the lost spacecraft/scicncc. A second project tradeoff to consider when offsetting the cost of SFT is the avoided cost of redesign if SFT was not done, but a serious failure mode was found late in the development cycle requiring design changes to prevent it from occurring.

### 3.1 Effectiveness Versus Failure Modes

As mentioned in section 2.1.1, SFTs do not avoid any specific failure mode, but do depict and facilitate an understanding of all known failure modes and interactions between elements of the spacecraft. "l'he SFT model development, if done rigorously, increases the chance of launching a spacecraft with no unidentified or inadequately mitigated failure mode. It should be acknowledged that neither SFT nor any other form of analysis can be guaranteed to identify all possible failure modes. However, SFTs are very effective tools for systematically analyzing, documenting and communicating information about failure modes and their mitigation on both simple and complex systems.

### 3.2 Sensitivities

SFT methods arc straight forward, but accurately representing a spacecraft design requires a somewhat unique combination of System Engineering, Software Engineering and the failure mode analysis skills of a Reliability Engineer. If personnel possessing the relevant skills are assigned to, the task, very complex spacecraft, such as Cassini, can be accurately represented at a cost of two to three work years. otherwise, the cost could be substantially higher and the resulting model could be of much less value. In summary, the most important parameters arc the S1 'T anai yst and the design information available to develop the model. Other parameters that influence types of failure modes detected by the SFT and the cost of performing the SFT are. identified in "l'able 1.

'1'able 1. Control Parameter Sensitivity and Cost Sensitivity

| Requirement | Control Parameters (P) | Effectiveness (E) vs Failure Modes (generic, specific) for default parameters | Parametric Sensitivity (dE/dP) + more effective 0 neutral - less effective | | | | | | | | | | | Cost Function (p) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| System Level Fault Tree | S/C Complexity (CX) | | | | | | | | | | | | | S/C Complexity (CX) |
| | Link to S/S FMECA (FL) | | | | | | | | | | | | | Link to S/S FMECA( FL) |
| | No. Dev Partners (N) | | CX | FL | N | MP | ML | SI | MR | TS | DM | FP | SW | No. Dev Partners (N) |
| | Mission Phases (MP) | | | | | | | | | | | | | Mission Phases (MP) |
| | Mission Life (ML) | Interface Errors | + | - | + | + | + | + | + | + | - | - | - | Mission Life (ML) |
| | No. Science Instru (S1) | | | | | | | | | | | | | No. Science Instru) (SI |
| | Margins [Pwr, Men, Mass] (MR) | Un-ID'd S/S Funct Failures | + | - | + | + | + | + | + | + | - | - | - | Margins [Pwr, Men, Mass] (MR) |
| | Dev Team Size (TS) | Un-ID'd S/S Part Failures | + | - | + | + | + | + | 0 | 0 | - | 0 | 0 | Dev Team Size (TS) |
| | Dev Mode [C.Eng] (DM) | | | | | | | | | | | | | Dev Mode [C.Eng] (DM) |
| | Fault Protection (FP) | | | | | | | | | | | | | Fault Protection (FP) |
| | S/W IV&V (SW) | | | | | | | | | | | | | S/W IV&V (SW) |

## 4.0 References


1. JPL 11-5703, "Jet I'repulsion laboratory, Reliability Analyses Handbook", prepared by Projec Reliability Group, July 1990.

# 6. Electronic Parts .Stress Analysis

## 1.0 Objectives

The highest level objective is developing spacecraft which meet the reliability expectations of a specific program. One of the activities used to assure high reliability of electronic circuits is derating of the circuit components to reduce. their failure rates. Derating provides the circuit components with reduced failure rate and robustness, so if unexpected conditions (e.g. increased duty cycle, warmer than expected operating temperatures, etc.) develop, the components will not fail prcnlaturcly.The objective of reducing failure rates of electronic circuit components during space. missions is achieved when the. lower level objective of validating, via Part Stress Analysis (l'SA), that the design meets the parts derating criteria is met.

## 2.0 Typical Requirements

Perform electrical circuit anal ysis on all electronic and electromechanical hardware to validate that st ress levels on circuit components comply with derat ing req ui rements, under worst case conditions. The electronic PSA is supported by a piece part thermal analysis. Guidelines for performing PSA arc provided in JPL D-5703, (Ref. 1 ).

### 2.1 Rationale

Electronic circuit components are prone to early failure when overstressed, (i.e., excessive power dissipation, high current, over voltage., high junction temperatures, etc.). Conversely, reduced failure rates can be achieved by reducing circuit component stress levels by design practices that reduce stress levels. Reducing circuit component stress levels has become well developed and is called "Derating". Electronic PSA verifies compliance with the derating requirements. The guidelines in J]']. D-5703 arc provided to promote uniformity of analysis methods used by various hardware suppliers, within and across various projects.

#### 2.1.1 Relevant Failure Modes

Typical relevant failure modes are:

1. Design, Parts, Parts Stress/SclcctionNJcar out/Aging.
2. Design, Life, Deterioration/Randon~ Failure.

Note: Not included in this miniproduct arc unacceptable functional failures duc to component degradation with age and stress levels. These functional failures arc addressed in the circuit Worst Case Analysis (WCA).

#### 2.1.2 Supporting Data

As indicated in Section 3.1, I'SA is virtually the only gate that validates that components in the cIcctrical/electronic circuit comply wit h their derat ing requirements. This is manifested by the lack of J]']. ground testing PFRs that arc related to overstressed components. in addition, there arc no known inflight failure on JPL programs that were linked to component overstress. Only a fcw ground testing problems have been linked to errors in the derating validation as indicated in the '1'able 1.

| Table I. OVER STRESS RELATED PFRs of JPL's MISSIONS | | | |
|---|---|---|---|
| Program | Year | Subsystem | Failure mode |
| Mars Observer | 1991 | Camera | Over-voltage to transistor |
| Sir-C | 1992 | Replay/Slow Control Unit | Overstress of Opto-Isolators |
| Sir-C | 1993 | RF Electronics | Over current through relay contacts |

## 2.2 Methods

Electronic PSA uses electrical circuit analysis to verify that the circuits' components comply with the derating requirements of Mil-Std-975, Appendix A, under all expected operating conditions, including short term transients associated with on/off switching, mode changes, etc. In most cases, the PSA (and the circuit Worst Case Analysis) require a supporting piece part thermal analysis. To simplify the analysis and provide a conservative design, the PSA is done using worse case assumptions. These assumptions include: 1 ) initial component variations, 2) environmental extremes plus margins, especially ambient temperatures, the thermal rise to the component and component internal thermal rise, 3) input variations plus margins, including voltages, currents, frequency, and duty cycle, and 4) outputs, including variations in load impedance. Guidelines for performing PSA arc documented in JPL D-5703. It should be noted that PSA does not address protecting, circuit components from the transient effects of Electrostatic Discharge (ESD).

## 3.0 Tradeoffs

Since most stress related early failures arc not detectable in the normal ground testing program, the PSA tradeoff evaluation considers the cost of performing the analysis versus a reduction in expected cost (in a probabilistic sense) of a premature failure during the mission by avoiding overstressed circuit component parts. Specifically, the actual cost of providing the PSA is compared to the change in expected cost of an premature inflight failure. The latter is based on the change in the probability y of premature in flight fai lure, the fraction of the mission lost and the monetary value of the lost SpaCCCraft science. Another issue to consider when offsetting the cost of the PSA is the avoided cost of redesign that might be required if overstressed circuit components are discovered late in the development cycle.

## 3.1 Effectiveness Versus Failure Modes

I'SA is very effective in avoiding over-stress in electronic circuit components and the associated premature failures during the mission. In fact, the PSA is virtually the only gate that validates the designer's nominal circuit design complies with the derating requirement during adverse conditions. Stated another way, there arc no other activities, including tests which validate that circuit components meet their derating requirements. Consequently there is no way of verifying that the circuits components will survive for the duration of the mission. Accelerated testing at elevated temperatures could be used to identify the "weak link" in the circuit components, but this approach does not directly reveal information about the other circuit components, so it has not been used extensively.

## 3.2 Sensitivities

The sensitivity of premature mission failures to "doing/not doing" PSA is potentially significant, unless the original circuit design includes the validation that circuit components meet their derating requirements under equivalent PSA conditions. '1'here is a monetary cost associated with expanding the basic circuit analysis to include the derating validation, but that cost should be less than a separate PSA performed by a different analyst. ~'able 1 I identifies PSA parameters and their influence on failure modes detection and the cost of performing PSA.

'T'able II. Control Parameter Sensitivity and Cost Sensitivity

| 'ontrol Parameters P) | ffectiveness (E) vs ailure Modes eneric, specific) for efault parameters | 'arametric Sensitivity (dE/dP) + more effective 0 neutral - less effective | | | | | | | ost Function (p) | |
|---|---|---|---|---|---|---|---|---|---|---|
| ircuit Complexity CC) | ver Stressed Components | CC | QT | FA | DT | ML | DC | A | ircuit Complexity (CC) | + |
| ual Temp (QT) | -Electromigration | + | + | + | 0 | + | + | + | ual Temp (QT) | 0 |
| light Allow Temp FA) | -Interface Diffusion | + | + | + | + | + | + | + | light Allow Temp (FA) | 0 |
| elta-T [S.I'late-I'ar[] DT) | -Dopant Migration | 0 | + | + | + | + | + | + | elta-T [S.I'late-I'arl] (DT) | |
| lission Life (ML) | -Over temp of Components | + | + | + | + | 0 | 0 | 0 | lission Life (ML) | + |
| ktDuty Cycle (DC) | -Phase Change | + | + | + | + | 0 | − | 0 | kt Duty Cycle (DC) | 0 |
| SS vs EVA (A) | -Out Gassing | + | + | + | + | 0 | 0 | 0 | SS vs EVA (A) | + |
| | erformance Degradation | | | | | | − | | | |
| | -Timing | + | + | + | + | + | + | + | | |
| | -Output Voltage | + | + | + | + | + | + | + | | − |

## 4.0 References

1. JPL 11-5703, "Jet Propulsion Laboratory, Reliability Analyses Handbook", prepared by Project Reliability Group, July 1990.

# 7. Unit Level Temperature Design Requirement

## 1.0 Objectives

Design requirements are used to ensure that the hardware is designed, built, and tested to be compatible with the spacecraft, as well as with other hardware. Temperature design requirements are used to ensure that the assembly (unit) will operate as intended over the range of mission environments seen during its life, including assembly, test, and launch operations.

Design requirements usually include margin beyond the intended use environment. These margins are used to account for any differences between the ground activities and the mission environment. They are also intended to provide a buffer for variations in the intended application, inherent uncertainties in the predicted mission temperatures, and to provide for testability at higher levels of integration.

The temperature design requirements need to be compatible with the thermal test requirements, since the thermal tests are a critical part of the overall reliability demonstration for an assembly (unit ). A typical set of temperature design requirements has the widest temperature ranges at the assembly (unit) level, with gradually narrowing range for the subsystem, and finally system levels. This ensures that the assemblies are robust enough for their application, and that their capabilities are used outside what they will be subjected to on the spacecraft. This not only increases confidence in the reliability of the assembly (unit), but it also results in available flexibility in mission operations if the available margin is known.

## 2(.0 Typical Requirements

The typical temperature design requirements consist of the. following components: 1 ) operating temperature range; 2) non-operating temperature range; and sometimes: 3) survival temperature range; and 4) in-spec operation temperature range.

These parameters address the needs and uniqueness of each assembly (unit) and mission. The temperature design requirements must be coordinated with the thermal test requirements for the assembly. The design requirements must, at minimum, encompass the expected test temperatures (which, in turn, encompass all the temperatures seen throughout the life of an assembly).

### Operating Temperature Range

The operating temperature range. is the range over which the assembly (unit) must operate and meet the applicable functional requirements. This range is typically -20 to 75 °C or greater, and provides compatibility with the thermal test requirements for the assembly (unit), anti minimizes problems when testing at higher levels of assembly.

### Non-operating Temperature Range

The non-operating range is often the same as the operating temperature range above. However, it can be. used to define 'survival extremes' (see below). If the operating temperature range encompasses all operating and non-operating scenarios for the assembly (unit), the non-op range is not used. If the assembly (unit) is expected to be powered off for some conditions, then a non-operating range can be defined which is wider than the operating temperature range. The assembly is designed to turn on safely at the extremes of the non-operating temperature range, and return to in-spec. functional performance as the temperatures return to the operating range. This allows for S/C safing modes, loss of attitude control, and other modes in which the assembly (unit) is not required to operate within specified functional requirements. This requirement is mission specific.

**Survival Temperature Range**

A survival temperature range is occasionally specified. This is usually defined as an extreme temperature that the assembly (unit) can be exposed to, yet turn on and operate without degradation after returning to a more benign state. Survival temperature requirements mostly affect the rupture, or hysteresis failure modes, encompassing mechanical, packaging, and tolerances within an assembly (unit). Fluid filled devices, or other devices relying on scaling must retain their integrity in such a condition. Survival temperature requirements are mission specific.

**In-specification operating Temperature Range**

In designing assemblies for space use, certain technologies exhibit temperature dependence that make it prohibitive to expect compliance with all functional specifications over a wide temperature range. Typical of these are RF systems, optics, and some mechanisms. In order to accommodate this, these types of assemblies are usually devoted special resources in the system design to maintain them within a tighter temperature range than other subsystems. Correspondingly, the temperature design requirements can specify a narrower range in which in-specification operation is required. The performance is allowed to degrade outside this narrower range. This performance degradation, however, is expected to be predictable and repeatable, returning to a stable, in-spec functional state as the temperature returns to the specified range. This requirement is usually an addendum to the operating temperature requirement, and it varies on a case by case basis. However, typical in-spec temperature ranges have been 5 to 55 °C for some recent projects.

## 2.1 Rationale

Temperature affects most mechanical anti electrical designs due to material property dependencies on temperature, temperature induced tolerance changes, and temperature effects on electronic device parameters. These effects must be accounted for in the design of structures, mechanisms, and circuits in order for the design to function as intended when exposed to the various temperature regimes seen throughout the life of an assembly (unit).

### 2.1.1 Relevant Failure Modes

Sonic temperature induced effects on assemblies are listed by type:

**Structures (both macro and micro):**

1. Subject to internal stresses due to temperature and CTE (coefficient of thermal expansion) mismatches - these can result in either rupture, unwanted de. format ion, or car] y fat igue failure. These stresses can be residual due to processing history, or can be induced by the operating environment.
2. Low cycle fatigue can be induced by cyclic temperature variations. Primarily seen in electronic interconnects such as vias and solder joints.
3. Interfacial stresses can result in cracking and failure of bonded joints, or in cracking or delaminat ion of the materials on either Side of a bonded joint.

**Electronics:**

1. Functional failures can be experienced due to electronic component parameter variat ions which are temperature dependent, Examples are: transistor gain, diode forward current, CMOS switching speed (and hence power dissipation) variations, timing margins, and voltage thresholds, among others.
2. Start-Lip transient conditions such as excessive inrush current can be caused by temperature effects on the components.
3. Device failure mechanisms such as electromigration and time dependent dielectric breakdown, among others are accelerated to varying extents by temperature. For failure mechanisms with positive activation energies (those just mentioned), extended high temperature operation will

lead to early device failure. Conversely, for failure mechanisms with negative activation energies, such as hot carrier inject ion, cold temperatures wil 1 accelerate the failure mechanism.
4. Extreme temperature conditions can also combine with electrical parameters to result in part overstress.

**Mechanisms;**
1. '1 'olerance variations due to CTE effects.
2. Variation in motor torque output and current draw.
3. Fluid viscosity and density changes that can lead to leakage, deformation, or undesired operational characteristics.

**Optics**
Optical systems arc typically sensitive to temperature. variations. Performance of reflective optics is dependent on the distance between and alignment of optically reflective surfaces. Dimensional changes wil 1 affect the focal point of the system. Refractive optics have additional sensitivities due to the variation of the index of refraction with temperature. Low CTE materials arc used to minimize dimensional changes, and lens and mirror mounts must accommodate dimensional changes without inducing large stresses in the optical elements. Residual stresses in the materials due to machining can aggravate the temperature sensitivity of optical structures. optical coatings and filters are usual 1 y sensitive to temperature, indicated be either performance changes, or accelerat ed degradat i on.

**Synergism**
Since so many electronic and optical parameters are. affected by temperature, derating guidelines have been developed by the industry to enhance the life and reliability of electronic parts under various applications. When establishing design temperatures for electronic assemblies, it is import ant to work c1oscI y with the environmental compat ibi lit y, reliability, and parts experts to est at-i] ish a coherent policy for the project which performs the t radeoffs necessary to arrive at an optimal set of design and test requirements. The. same holds true for other types of assemblies. An apparent] y more restrictive requirement on one assembly (unit) may result in a much more relaxed requirement on a system. The subsystem and system must be considered when deciding on the assembly (unit) requirements, in order to avoid decisions which will result in unnecessary constraints on other assemblies, or higher levels of integration.

### 2.1.2 Supporting Data

One measure of the effectiveness of designs to accommodate the necessary temperature ranges is to examine the number of design related problems found in the test program. Although design problems arc not indicators of the effectiveness of the requirement, they do point to the need for a designer to be aware of and adequately address the temperature effects on a given assembly (unit).

The P/FR database was searched to find P/FRs generated during thermal tests, and among these, to isolate design related P/FRs. The projects searched included Galileo, Mars observer, Topex, MGS, NSCAT, SeaWinds, Cassini, MISR, and Mars Pathfinder.

The search priorities were: for the environment, temperature; and for the cause, design. Out of 775 total P/FRs for these projects, 130 (17%)) of them satisfied the search criteria of originating during various temperature environments, and the cause attributed to design issues. 'l'able. 1, below shows the 130 P/FRs broken down by type of design problem.

**Table 1 - Distribution of Design Related P/FRs by Cause**

| Cause of Failure | Number of Occurrences | Percentage of Total |
|---|---|---|
| Design (unspecified) | 44 | 34 |
| Functional Application | 27 | 21 |
| Packaging/Mounting | 7 | 5.5 |
| Producibility | 24 | 18 |
| Parts/Materials Misapplication | 21 | 16 |
| Tolerance Call-out | 7 | 5.5 |
| Total | 130 | 100% |

It is clear that a design requirement alone does not result in a good design, however, the requirement creates the awareness that temperature issues need to be accounted for in the design. It can be seen from the table above, that no one particular design problem dominates the types of failures observed. It is interesting to note that these design problems range from packaging and materials issues to specifications issues.

A close scrutiny of the P/FRs found that of the 130 initially flagged, 36 were not attributable to temperature effects, reducing the total related to design problems found during temperature testing to 94 out of 775, or 12%. The distribution of failures by design type remains approximately the same.

## 3.0 Tradeoffs

"Jim temperature design requirement is necessarily tied to the temperature test requirement. The design must, at minimum, accommodate the qualification temperatures. Given this, it is more appropriate to make the tradeoffs on the test requirements. The assembly (unit) temperature test requirement write-up will address the tradeoffs that can be made in that area.

One trade-off that can be made is in the system design. The project and the system architects should carefully consider the tradeoffs between system level and assembly (unit) level requirements. Often the decision is made to restrict the operating temperature range of the assemblies in order to realize cost savings in procuring the assemblies. In considering such a decision, the project should be sure that the restricted temperature range would result in real cost savings at the assembly (unit) level. The project should also evaluate the resulting impact on the system level design due to increased constraints on the system level thermal control, which can result in increased mass, heater power requirements, and constrained equipment layout.

## 3.1 Sensitivities

in establishing temperature design requirements for assemblies, the parameters that can be varied are: temperature, in-spec operating range, and survival (or non-operating range). Table 2, below, attempts to show the impact of changes in these parameters to: 1 ) the effectiveness in mitigating the failure mechanisms discussed above; and 2) the cost of the assembly (unit).

**Table 2 - Control Parameter, Sensitivity and Cost Sensitivity.**

| Control Parameters | Failure Modes | Sensitivity to Parameter | | | Cost Sensitivity to Control Parameter | |
|---|---|---|---|---|---|---|
| | | T | in spec | surv | | |
| Temperature Levels (T) | Structural/packaging | + | + | + | Temperature Level | 0 (1) |
| in-spec Range (in spec) | Electrical performance /parameter variation | + | + | 0 | in-spec Range | 0 (1) |
| Survival Range (surv) | Optical performance | + | + | 0 (2) | Survival Range | 0 (3) |
| | Time dependent failures (Arrhenius) | + | 0 | 0 | | |
| | | | | | | |

Notes:
1) Not a cost driver overt ypical temperature ranges (-20/+70 °C). RF ancl optics assemblies may have cost impact due to strong temperature sensitivity of their performance.
2) Survival temperature is not a driver, unless the range is wide enough to cause permanent change in the optics structure.
3) Not a cost driver unless effect mentioned in (2) is an issue.

Temperature design requirements, while not guaranteeing a quality design, do define many issues to be addressed during the. design process. Tolerances, material compatibility, electrical parameter variations, and functional requirements all need to be considered when designing to operate in a given environment. It is also important to note that the temperature design requirements need to be closely tied to the test requirements, as well as the part stress analysis, derating, and worst case anal ysis requirements in order to assure consistent application of environment al require ments.

# 8. Unit Level Thermal Test Requirement

## 1.0 Objec tives

The objective of unit level thermal testing is to demonstrate the flight worthiness of the hardware. 'l'his is done by simulating the relevant synergistic environmental and operational conditions through selection of appropriate combinations of environmental, electrical and mechanical parameters. To be effective, parameters should be selected that validate the design, demonstrate its robustness, screen for workmanship defects, and demonstrate an acceptable level of reliability. Thermal tests are designed 10 be non-destructive and arc performed under either vacuum or atmospheric pressure conditions.

## 2.0 **Typical** Requirements

The typical unit level test requirement consists of the following parameters: test pressure, operating temperature range, non-operating temperature range, dwell times, temperature transition rates, number of temperature cycles, and functional testing.

These parameters are chosen to best achieve the test objectives for a given unit and mission. The test parameters arc necessaril y synergist ic with the temperature design parameters for the unit, and must encompass all the temperature regimes experienced t hroughout the life of the unit. These parameters will be discussed in more detail in section 2.1, outlining the effect o: these parameters on the fai lure mechanisms involved and on the effect iveness of the test.

A typical unit thermal test requirement is:
1 Iot/Cold Temperature Level (operating): -20/+75 °C
Hot/Cold Duration: 144/24 hrs
Number of Cycles: ]
Pressure: <10-S Torr
Rate of Change of Temperature: 30 °C/hr
Functional Testing: to demonstrate in-spec operation over a temp range

This example is typical of traditional test requirements for assemblies used in long life planetary exploration missions. These requirements arc tailored as mission requirements anti program needs change.

## 2.1 Rationale

A well designed and implemented thermal vacuum test can expose most of the relevant failure modes. Published data shows that thermal vacuum testing is the most effective environmental test for space hardware. The following is a discussion of the rationale for the significant variables that affect the effectiveness of a thermal vacuum test.

**Functional Testing**: Functional tests arc necessary to verify the performance of the hardware during environmental testing. Electrical stresses arc combined with environmental stresses to effectively apply screening stresses to the hardware under test. Because of the synergism between the electrical and thermally induced stresses, the effectiveness of an environmental test can be significantly influenced by the selection and performance of various functional tests during the environmental test. Functional tests should be designed to allow verification of unit level functional requirements, including in-specification operation of all modes over the full operational temperature range, stability, calibration, and demonstration of cold- and hot-start capability. in many cases, out of specification operation at or near the extremes of the temperature range is

acceptable as long as the performance comes back in specification within the required range, and no permanent degradation occurs.

**Test** Pressure: The pressure during test results in both thermal effects as well as purely pressure dependent phenomena. The effects associated purely with pressure include corona and multipacting. These arc most often associated with RF or high voltage circuits and devices. Introduction of a gas to the test environment (even fractions of an atmosphere) introduces addit ional heat transfer via convection, which alters the temperature distribution within the unit. Therefore, the vacuum (< 10-s '1'err) environment is most representative of flight for unit thermal tests. 1 lowever, testing in a dry 1 atmosphere environment is acceptable if it has been shown that the hardware is not subject to corona and multipacting, and the internal temperature levels have been calculated and can be achieved by adjusting the test temperatures.

**Temperature Level**: For most failure mechanisms associated with space flight electro-mechanical hardware, the hot temperature level is one of the key parameters impacting the effect i veness of the then nal test. In general, the higher the level the more perceptive the test (Reference 3). Cold exposures arc effective in precipitating many latent failure modes, and complement high temperature exposures. These levels have typically been the greater of -20/+ 7s °C, or 25 °C beyond the worst case predictions, These levels assure robust screening of the hardware, in addition to providing adequate margins to account for environmental and modeling uncertainties.

**Duration**: The reliability y of an electronic unit in flight is directly related to the number of operat ing hours experienced prior to flight. Additionally, since increased temperature accelerates many failure mechanisms, the time spent operating at elevated test temperatures is equivalent to a greater time spent operating at lower temperatures. The test dwell time can be traded off for increased operating time in other environments. However, since realistic accelerat ion factors must be used, this tradeoff should only be done after consulting with the project reliability engineer. Non-operating dwell times are not necessary unless the hardware is subjected to a hystcres]s-type of mechani sm.

Rate of **Change in** temperature **(dT/dt):** At high rates of change in temperature, large stresses can build up across material interfaces due to differential thermal expansion which can be significant enough to cause a failure of the material, 'l-here is concern that a excessive rate of change in temperature could cause possible failures which would not have occurred in flight. The current approach is to specify a rate of temperature change which is tied to the maximum rate expected in flight, The rationale for this is that any savings associated with a higher rate would be insignificant and this would subject the hardware to levels that could be in excess of any previous qualification rates. The allowed rate of change in temperature is dependent on the design and previous qualification of the hardware. Typical electronic packaging designs used for space applications should be capable of supporting rates in the range. of 10°C/minute.

**Temperature** Stabilization: Thermal stabilization is important when the hardware under test has an extremely long thermal time constant (time to reach thermal equilibrium), uses localized internal temperature control, or where hysteresis phenomenon is invol ved,

Number of' Thermal Cycles: Performing a single thermal cycle is effective for precipitating a broad spectrum Of latent defects, These range from workmanship defects (poor interconnect integrity, missing parts, wrong part value, etc. ) to electrical, optical and mechanical design defects, Performing mu ltiple thermal cycles is effective in testing for hysteresis effects and life testing (such as qualifying the capabilities of a technology). Since. life testing is not intended to be part of a test on flight hardware, the number of cycles should be the minimum number necessary to verify stability anti/or repeatability in performance.

**Heat** Sinking **Method**: Heat sinking the unit under test in the same manner as in flight aides in the detection of any deficiencies in the thermal coupling of the. unit to the next level of integration.

### 2.1.1 Failure Mechanisms & Tradeoffs

For the purpose of this discussion, all failure mechanisms are grouped into one of three general classifications. They are: 1) chemical/diffusion mechanisms (Arrhenius reaction rates); 2) hysteresis; and 3) stress rupture. A high-level summary of each of these classifications is presented below. Each discussion is followed by a list of the test parameters that influence that failure mode.

**Chemical/Diffusion** Reactions

The. fabrication of electronic parts, circuit boards and circuit-board assemblies involves complex chemical reactions. Failures as a result of residual reactants, incomplete reactions or diffusion/migration processes would be classified as being Arrhenius in nature. This failure mode is most often associated with electronic parts (Reference 1). Moreover, Reference 1 also indicates that this mechanism can be the leading source of failures for a significant number of other hardware elements.

Relevant test parameters (listed in estimated order of overall significance) are:
Electrical loads, Hot Levels (including pressure level effects), Hot Dwell Time, Cold Levels, Cold Dwell Time, Ramp Rate.

**Hysteresis**

The forms of hysteresis most often of concern in clcctro-mechanical hardware used in space flight are: fatigue (both high and low cycle) and parametric drift. Low cycle fatigue and parametric drift arc a function of dwell time and number of cycles,

High Cycle Fatigue: high cycle fatigue failures are best exposed by vibration testing and therefore not discussed herein.

Low Cycle Fatigue: The life-limiting failure mechanism of typical packaging designs is low cycle fatigue of electro/structural interconnects. This damage mechanism largely results from a global mismatch of the CTE between: (1) part body and the board it is mounted on, (2) the board and the board housing. local CTE mismatches (between solder material and metal pad on the board) also contribute. to the problem. Similar problems occur in materials with the same CTE's but where large thermal gradients "exist within the solder joint/lead system.

The material properties which govern the life of solder interconnects are very non-linear (Reference 3). As a result, cyclic exposures which involve higher peak thermal exposures arc significantly more effective than cyclic exposures of the same total depth but which involve. a lower hot peak temperature. Moreover, below 0°C, eutectic tin/lead solder becomes significantly stronger, and thereby, most likely changes the failure mode for the interconnect from a low cycle fatigue failure. of the solder material to a brittle failure of either the solder material or the part package.

Parametric Drift: Another form of hysteresis is parametric drift. It can be due to Arrhenius type react ions or residual stress effects, Thermal cycling general 1 y removes/stabilizes these stresses.

Relevant thermal test parameters (listed in estimated order of overall significance) arc:
Hot level, total depth of thermal cycle, cold level, hot dwell time, electrical loads, ramp rate, Pressure level.

Stress **Rupture**

Stress rupture failure can be introduced via mechanical loading or thermal displacement as a result of a CTE mismatch or large thermal gradients. Excursions away from the zero stress and/or residual stress state (associated with the formation/fabrication processes) create stresses in the hardware. Most stress ruptures arc suspected to occur as a result of manufacturing flaws or ncw designs. This is a typical weak link failure mode for bondlines and composites.

Relevant thermal test parameters (listed in estimated order of overall significance) arc:
Hot & Cold Levels, Electrical loads, Pressure level, Ramp Rate.

### 2.1.2 Supporting Data

Studies of test results indicate that the thermal vacuum test is the most flight-like environment achievable prior to launch, and it is the most effective environmental test for revealing inherent failure, modes (Reference 4).

The following data is based on studies of the JPL Problcnl/Failure Report (P/FR) database, and summarize test experience on major JPL flight projects.

General Effectiveness of Thermal-Vacuum Test: Anal ysis of the data shows that approximately 25% to 30% of the problems found during testing of flight assemblies on the Voyager and Galileo programs would not have been detected except by environmental testing. Additional studies were conducted to compare the relative effectiveness of the two major environments, vibration tests and thermal tests, These studies found that thermal testing detects from 1.3 to 3 times as many problems as dynamics testing. Scc Reference 6 (TO-0003) for further details.

Effectiveness of Functional Tests: Two spacecraft (Galileo and TOPEX/POSEIDON) and two instruments (the Wide Field & Planetary Camera 11 ( WF/PCI I) and the NASA Scatterometer (NSCAT)) were st udied by performing a trend analysis of the problem/failures detected during system level thermal/vacuum testing to provide some insight on the role and effectiveness of functional testing. Table 1 summarizes the findings of this study. Of 20 PFs relevant to the study, 40% (8) should have been detected during lower level testing. Conversely, 35% (7) involved "interface issues" which could only be resolved by higher level testing. The remaining 25% (5) were detected during lower level testing but were not effectively resolved to prevent future occurrence. Scc Reference 7 (TO-002.7) for further details,

**Table 1. Summary of Functional Test Effectiveness observations**

| CLASS1FJCATION OF PF DETECTION | SPACECRAFT | INSTRUMENTS | TOTAL |
|---|---|---|---|
| Undetectable At Lower integration Level | 7 | 0 | 7 |
| Potentially Ineffective Problem Resolution | 3 | 2 | 5 |
| Potentially Ineffective Functional Testing At Unit Level | 4 | 4 | 8 |
| TOTALS | 14 | 6 | 20 |

Effectiveness of Vacuum: The use of vacuum conditions during thermal testing of hardware can significantly increase the effectiveness of the thermal test as a screen for detecting hardware defects. References 2 and 4 report that thermal/vacuum testing is more effective for revealing defects than thermal/atmospheric testing.

Reference 8 documents a survey made of the P/FRs written during unit level and system level thermal/vacuum (T/V) tests for the Voyager and Galileo Projects (pre-1986) to determine. the necessit y of a vacuum environment along with elevated temperat urc for uncovering P/F's. Tables 2 and 3 summarize the unit and system level findings of this study, respectively. Note that on both programs and both levels of testing, vacuum effects played a major role in detecting the problcnl/failure.

Table 2. Unit-1 .evel TV Test

| DEPENDENCY | VOYAGER | | GAI .11.130 | |
|---|---|---|---|---|
| | NUMBER | PERCENT | NUMBER | PERCENT |
| Temperature Only | 9 | 19.6 | 7 | 19.4 |
| Temperature & Vacuum | 10 | **21.7** | 17 | **47.2** |
| "Pure" V a c u u m | 21 | 45.7 | 8 | - 2 2 . 2 |
| Indeterminate | 4 | 8.7 | 3 | 8.3 |
| Other (functional only, etc.) | 2 | 4.3 | 1 | 2.8 |
| **TOTALS** | 46 | **100** | **36** | **100** |

**Table 3. System-Level TV Test**

| DEPENDENCY | VOYAGER | | GALILEO | |
|---|---|---|---|---|
| | NUMBER | PERCENT | NUMBER | PERCENT |
| Temperature only | 0 | 0 | 4 | 10.3 |
| Temperat urc & Vacuum | 6 | 13 | 5 | 12.8 |
| "Pure" Vacuum | 29 | 63 | 14 | 35.9 |
| Indeterminate | 2 | 4.3 | 2 | 5.1 |
| Other (functional only, etc.) | 9 | 19.6 | 14 | 35.9 |
| **TOTALS** | **46** | **100** | **39** | **100** |

Hot 1 .evel and Dwell Period: Exposure, to high temperature testing has been found to be effective in revealing design and workmanship defects. Precipitation of latent defects associated with all three t ypes of failure mechanisms discussed in section 2.1.1 is accelerated by exposures to hot levels (Reference 3). Although time itself is not an acceleration mechanism, it increases the probability of detecting a latent defect during the test. Table 4 summarizes several examples of PFs that were temperature level and or time dependent. These findings arc from a study performed to

investigate and document specific examples of PFs which were dependent on high temperature exposures and/or time at high temperature. (See Reference 9 for further details.)

**Table 4 - Causes and Mechanisms of Thermal Vacuum Hot Test Failures for Galile**

| PFR # | Failure Description | Failure Mechanism | Failure Physics | Time (hr) | Temp (°C) |
|---|---|---|---|---|---|
| 43996 | T/V test data output became intermittent. | Three pins were not soldered to circuit traces. | Hot temperature caused expansion leading to the discovery of un-soldered pins. | 10 | 55 |
| 42485 | Memory errors found while debugging (ref PFR 42492). | Breakdown in gate oxide of one of the memory transistors. | Most probably a ESD latent defect. | 83 | 75 |
| 42493 | Excess current detected in memory array(ref PFR 42492). | Breakdown in gate oxide of one of the memory transistors, | Most probably a ESD latent defect. | 186 | 74 |
| 42494 | control failure found in trouble shooting (ref PFR 42493 ). | Breakdown in gate oxide of one of the memory transistors. | Most probably a ESD latent defect. | 143 | 75 |
| 42495 | Missing interrupt and no response to iso-valve (ref PFR 42492). | Breakdown in gate oxide of one of the memory transistors. | Most probably a ESD latent defect. | 145 | 75 |
| 43283 | Memory array supply voltage out of spec. | Short between 10 V & Gnd layer at the positive terminal. | Failure to correct for laminate shrinkage when terminal holes were drilled causing breakdown of epoxy insulating material under voltage and thermally induced mechanical stress. | 155 | 75 |
| 43588 | Memory array read zero after PWR reapply. | Short between 10 V & Gnd layer at the positive terminal. | Same as 43283 above. | 32 | 75 |
| 44458 | Memory address failures on the AACS. | Solder bridge found was causing contention. | Expansion of board and/or conformal coat due to CTE effects, shifted entrapped solder particle such that the short occurred. | 102 | 55 |

Cold Level and Dwell Period: A study of PFR data indicates cold exposure is effective in uncovering design and workmanship PFs in piece parts, electronic circuits and mechanisms.

Table 5 indicates several very significant part problems which were first detected at the unit level. The cold piece part problems documented were arguably the most significant problem to occur on the Galileo Project. See Reference 10 for further details.

'1'able 5 - **Causes** and Mechanisms of Thermal Vacuum **Cold** Test Failures **for** Galileo

| PF # | Failure Descriptio | Failure Mode | Failure Physics | Role of 1 ow Temp. | Role of Test Time | Time (hrs) | emp (°C) |
|---|---|---|---|---|---|---|---|
| 400. | LGA-2 actuator ra to slow | Actuator ran to slow. | Viscosity of grease inversely proportional to temperature | Increased viscosity of grease to point where actuator was to slow | None | 62.4 | -60 |
| 4248 | ACE MEM/DM Memory failure | Gate oxide Breakdown | **Hot Electrons** (Note activation energy for this phenomenon is negative.) | Current stress is inversely proportional to temperature. **As** the current stress increases the rate of gale oxide breakdown increases, | Failure rate is time at cold temperature dependent. Therefore, cold dwell appropriate for screening these failure modes. | 7 | -15 |
| 4249 | Star scann MEM/DM had addres failures | Gate oxide Breakdown | **Hot Electrons** ( Note activation energy for this phenomenon is negative. ) | Current stress is inversely proportional to temperature. As the curi ent stress increases the rate of gate oxide breakdown increases. | Failure rate is time at cold temperature dependent. therefore, cold dwell appropriate for screening these failure modes. | 58 | 20 |
| 4259 | Star scann output wor count erro | Failure of signal lead | Unknown, but suspect thermally induce.d strain. | Unknown, but suspect thermal strain associated with cold level | None suspected. | 1].5 | -27 |
| 4419 | NIMS OA spectral measureme t shift | 1 VDT – sensitivity below specification | LVDT circuit sensitivity is a function of its natural frequency which in turn is a function of temperature | LVDT circuit sensitivity is proportional to temperature. | Not known, but assumed to be none time dependent | 26.5 | 108 |
| 4356 | Sunshade. Cover faile to deploy after pyre, firing | Excessive – cover preloac + lubrication failure | I lubrication scrubbed off during vib test, resulting in failure in thermal/vac | None associated with the failure that occurred. | **None** | 17 | 115 |
| 4498 | Read Disturb Problem in TCC244's | IC **design** – flaw & "Charge Pumping" | Row decoder transistor reach full turn on at low temperatures and high voltages | Transistor [urn-on time is shorter at cold thereby allowing charge pumping to take place. | **None.** However, This pattern sensitivity PF requires a significant number of pseudo-random data patterns to be tried in order to have a reasonable probability of detecting an error. | 10 | 20 |
| 5059 | Read Disturb Failure in 11 S6504 Device | Unable to discharge the column line to "O" duc to a poor contact bet wccn metalization & Vss | The electrical resistance of contact degraded due. to **electro-migration** while the alternative current discharge path s inversely proportional to temperature. | Electro-migration is accelerated by the higher current stresses associated with cold operation ANI) the leakage current increases as conductance increases with a decrease in temperature. | Degradation of the contact via electro-migration is time sensitive at cold | nitial Test It cold | 20C |

1 ;ffectiveness of Time Rate-Of-~han~c of Temperature (d'l'/clt): Historically, the rate of change during the thermal/vacuum test has been tied to the maximum rate expected in flight, This approach was taken because it has been demonstrated that some types of hardware are sensitive to high rates of change in temperature. A good example of this type of hardware arc solar panels. Hardware which is subjected to high rates of change in temperature during flight typically undergo some form of life/qualification testing to verify their flight worthiness. This type of testing tends to be costly. The selection of a temperature ramp rate to be used during a thermal test balances the cost savings (test time) versus the possibility of inducing unwanted failures by using too severe a ramp rate. The typical thermal test of electronic assemblies involves a single thermal cycle and therefore any potential cost saving would be insignificant. In light of this the typical rate specified for testing of bus electronics assemblies has been three times the maximum flight rate, ]n many cases this works out to be 30 °C/hr.

Relative Effectiveness Of Thermal Cycles: Thermal cycle data collected for various electronic and electro/mechanical components shows a large number of failures on the first thermal cycle relative to the second and subsequent cycles. This appears to apply universal] y to electronic and electro-mechanical assemblies that are thermal cycle tested. Furthermore, there is little improvement beyond the second cycle in the number of failures detected. The best fit curve (of cycles 2 and beyond) shows that improvement is occurring, but at a slow rate. Upon analysis, the failure distribution appears to be hi-modal, The failures found after the first cycle appear to belong to a different group of failures than those seen in the first cycle. This is particularly evident when curve fits arc made on the data, The majority of the temperature-change failures (ones which need exposure to a thermal cycle) are found in the first cycle, leading to the conclusion that subsequent cycles add little to further detection of these defects. The failure population for cycles 2 and beyond seems to be composed primarily of positive activation energy Arrhcnius-Reaction-Rate type failure mechanisms. The cycling does not add significantly to the effectiveness of the test for this type of failure mechanism. (See Reference 1 1 for more details.)

## 3.0 Tradeoffs

Tradeoffs can be made with each parameter involved in the thermal test: temperature levels, duration, test pressure, number of cycles, temperature ramp rates, and electrical testing. As discussed above, these parameters all impact the effectiveness of the test to varying degrees. Time in test can be traded for bench top operation, hot levels can be traded for operating time, atmospheric pressure can be traded for vacuum, etc. These tradeoffs arc best made with a solid understanding of test effectiveness and how it is impacted by various parameters,

### 3.1 Sensitivities

in establishing thermal test requirements for assemblies, the parameters that can be varied arc: temperature level, dwell times, pressure, electrical testing, number of cycles, and temperature ramp rate. Table 6 attempts to show the impact of changes in these parameters to: 1 ) the effectiveness in mitigating the failure mechanisms discussed above; and 2) the cost of the unit.

'l'able **6 - Control Parameter Sensitivity**

| Test Parameter | | Arrhenius Reaction FMs | | Hysteresis/Thermal Stress FMs | | Cost Sensitivity |
|---|---|---|---|---|---|---|
| | | Pos Ea (1) | Neg Ea (1) | Low Cycle Fatigue | Parameter Drift | |
| | | ++ | - | + | + | 0 (5) |
| Temp. Level | Hot | ++ | | + | + | 0 (5) |
| | cold | | ++ | + | + | o (5) |
| Dwell Time | Hot | + | | + | + | ++ |
| | cold | | ++ | | + | ++ |
| Pressure | Vacuum | ++ | | + | + | + |
| | Atm. | | ++ (2) | - (2) | ? | 0 |
| Electrical Test | Voltage Margin | ++ | ++ | + (2) | + | (6) |
| | Freq. Margin | ++ | ++ | + | + | (6) |
| | Power Cycles | ? | ? | + | + | (6) |
| Ramp Rate | | o | 0 | -/? | +/? | o |
| No. Of Cycles | | o | 0 | + (3) | -t (4) | ++ (7) |

(Effect of increasing parameter value: + increases effectiveness/cost, - decreases effectiveness/cost, O no effect)

Notes:
1) Ea: Activation Energy
2) Effect of the addition of a gaseous medium cold biases the temperature of the test article. Could result in reaching cold levels where specific failure mechanisms change.
3) Also consumes flight life.
4) However, only up to the point where change stops. Also consumes flight life.
5) Temperature level is not a cost drive unless is forces exceptional design considerations.
6) Small increase in cost related to test equipment, generally no great at the unit level.
7) Increases cost by increasing test time.

## 4.0 References


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# 9. Electronics Parts Destructive Physical Analysis

## 1.0 Objectives

The objective of destructive physical analysis (DPA) is to screen out parts with obvious defects and identify latent defects that could produce part (mission) failure at some later time. Most DPAs are performed on active devices, including diodes, transistors, micro circuits (integrated circuits), gate arrays and hybrids. On occasion, for special requirements, passive devices are also subjected to DPA.

## 2.0 Typical Requirements

The database of the Cassini electronic parts acquisition was used for this study, since the Parts Program Requirements Document PD 699-212 called for'1 00% DPA on all part lots (a total of 786) other than capacitors and resistors. The faster, better, cheaper missions such as the New Millennium require a review of what is an effective screen and what could be eliminated to meet the new requirements.

### 2.1 Rationale

A series of procedures to assess the acceptability of electronic parts for space flight use has evolved over a period of several decades. In the context of the Faster, Better, Cheaper mandate from our customer (NASA), these procedures are now being evaluated in terms of their effectiveness in providing mission threatening defect detection. Each of the procedures itemized in this report utilizes project time and money. This evaluation of their effectiveness is possible due to the availability of an extensive database on electronic parts acquisition, resident in the Electronic Parts Engineering Office. The goal is to provide project planners/designers with pragmatic guidelines to help determine what parts requirements can be modified or eliminated to save time and money and what risk (if any), is thereby incurred.

#### 2.1.1 Relevant Failure Modes

The major relevant failure modes are listed below:

1. Visually apparent external non conformance
2. Radiographic detection of foreign material in the package
3. Corrosive gasses inside the cavity
4. 1 lermetic seal leaks
5. Scanning electron microscope (SEM) detected fabrication flaws
6. Wire bond pull force specification failure
7. Die Bond shear force specification failure (attachment)

#### 2.1.2 Supporting Data

The following is a summary of the detailed data in Table I of the Appendix:

1. For the Cassini electronic parts acquisition program 786 DPAs were performed, 'l'here were a total of61 lots that failed onc or more of the DPA tests which represents approximately 8%.
2. Of the 61 failed lots, 32 were subjected to further analysis/tests and used as a result of MRB approval.
3. Five lots exhibited defects which resulted in being returned to the vendor. Ten lots were down graded to non flight status.

4. The use of DPA to determine suitability of a potential part for the Cassini mission resulted in eliminating five part types early, thereby saving possible redesign time and cost of unusable inventory.
5. As a result of the DPA process for Cassini, approximately 3% of the lots so tested were not used for flight.

### 2.2 Methods

The following test methods arc documented in the appropriate MIL STDs such as 883D. The. specific set of t csts is dictated by the part type and the package type. For example if there is no cavity, the hermeticity test is not used.

1. External Visual Examination (EV)
2. Radiographic Analysis (RE)
3. Residual Gas Analysis (RGA)
4. Hermeticity Testing (HERM)
    a) Fine Leak
    b) Gross Leak
5. Internal Visual Examination
    a) Low Power (LPIV)
    b) High power (HPIV)
6. Scanning Electron Microscope (SEM) Examination
7. Wire Bond Pull Test (WBT)
8. Die Shear (attachment) Test (DST)

## 3.0 Tradeoffs

For a mission such as Cassini, the full DPA procedure was required. Current costs for a DPA range from $500 to $S00 each. When the spacecraft at risk costs $1.2 billion, the DPA cost is cheap insurance against electronic part failure. For the faster, bet tcr, cheaper missions, there are several ways the time and cost of performing DPAs could be tailored. The trend toward small assemblies with fewer parts (ICs having increasing circuit function density), the use of commercial grade parts and emerging technology along with limited project funding will bring pressure to reduce costs and maximize. probability for success. The database cited here was the result of testing grade 1 parts which were to meet MIL SPEC Class S or the Source Control Drawing (SCD) equivalent. Most of the failed DPAs were on lots where the manufacturer was required to test for the failed parameter. Referring to Table I in the Appendix, this study suggests that:

1. Hermeticity testing was ineffective and is a candidate for elimination. The lots that failed this test were aria] yzed and used, indicating the specificat ion did not reflect the application.
2. Die attachment yields lit tle value (2 out of 786 lots).
3. Residual Gas Analysis (RGA) failures were uniformly determined to be usable for Cassini. RGA is a good candidate for elimination from the DPA procedure.
4. Wire bond testing only found 2 lots that were deemed un flight worthy out of 786 DPAs.

These four steps, combining time and charges account for over half the cost of a typical DPA. A ncw project may examine the results presented here and decide whether or not a shortened (tailored) DPA is appropriate, thereby reducing time and cost in the electronic parts acquisition process. Part classes of lesser grade down to commercial (depending on several variables) will probably produce significantly different statistics than those in this study. Studies on parts of lesser grade arc in process from several aspects and will result in up dated reports as the data becomes available. It is essential for each new nlission/instrument to carefully assess the parts requirements, balancing schedule, cost and the mission parameters. Early formation of a design team consisting

of the designer, parts specialist(s) anti a procurement specialist will maximize electronic parts acquisition.

The usc of lower grade or commercial off the shelf (COTS) electronic parts intuitively suggests DPA be required on all lots of active electronic parts, since as this study shows, even lots that have had full up S level screening still fail DPA at a 3% rate.

The faster, better, cheaper missions such as the Ncw Millennium, require a review of what is an effective screen and what could be changed (if anything) to meet the ncw require.rncnts. Several traditional steps in the DPA process might be eliminated for COTS. Plastic encapsulate.d parts will not usc hermeticity, RGA, bond pull, or dic shear testing. The study for this RTOP has shown that these four test were not very effective, even on parts with packages that have cavities.

### 3.1 Effectiveness Versus Failure Modes

Of all the failures noted, 3% were determined to be unsuitable (high risk) for flight USC. This means that their usc was judged to be potential cause for mission failure. For a mission of the Cassini type, the. cost of retrofitting could be significant in terms of both time and money. The DPA expenditure in this case is considered inexpensive insurance, The DPA findings also identified problems with 32 lots that were subjected to additional analysis and testing to provide confidence that they meet the Cassini reliability requirements. The usc of DPA early in the acquisition process resulted in the rejection of five part types that had been considered as candidates for Cassini. This step saved considerable time and cost by preventing design time as wc]] as procurement of parts that ult imatel y would not have been acceptable for this mission.

### 3.2 Sensitivities

The sensitivity of mission failure to each DPA test mode is some.what complex and dependent on a number of variables. Each mission duration, operating environment anti launch mode will determine the specific sensi t ivit ics to failure modes detected with DPAs. The standard DPA covers eight relevant failure modes as shown in paragraph 2.1.1 of this document. Table 11 reflects the results on the Cassini project lot acceptance for USC. It should be revised as PFRs arc received and analyzed,

**Table** 11. Control Parameter Sensitivity **and** Cost Sensitivity

| equ' nent: | Control Parameters | FAILURE MODE | Sensitivity to Defect Detection<br>+ More Effective<br>0 Neutral<br>- Less Effective | | | | | | | | | | | | | | | Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DPA | | | P | L | S | M | FM | HE | FL | GL | BW | DD | MF | V | DT | BP | BD | DB | |
| | External Visual Exam (EV) | Package (P) Leads (L) Seals (S) Marking (M) | + | + | + | + | - | - | - | - | - | - | - | - | - | - | - | - | + |
| | X-Ray Examination (RE) | Foreign Material (FM) | 0 | + | 0 | 0 | + | 0 | 0 | 0 | + | + | 0 | 0 | 0 | 0 | 0 | + | + |
| | Residual Gas Analysis (RGA) | H2O Excessive (HE) | + | 0 | + | 0 | + | + | - | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | + |
| | Hermeticity (HERM) | Fine Leak (FL) Gross Leak (GL) | + | 0 | + | 0 | 0 | 0 | + | + | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | + |
| | Internal Visual Exam | | | | | | | | | | | | | | | | | | + |
| | Low Power (LPIV) | Bond Wire (BW) Die Defect (DD) Foreign Material (FM) | 0 | + | + | + | + | 0 | 0 | 0 | + | + | - | - | - | 0 | 0 | 0 | + |
| | High Power (HPIV) | Metallization Flaws (MF) Voids (V) Dielectric Thin (DT) | 0 | + | + | 0 | + | 0 | 0 | 0 | + | + | - | - | - | 0 | 0 | 0 | + |
| | Scanning Electron Microscope (SEM) | Metalization Flaws (MF) Voids (V) Die Defect (DD) | 0 | + | + | 0 | + | 0 | 0 | 0 | + | + | + | + | + | + | + | + | + |
| | Wire Bond Testing (WBT) | Bond Pull (BP) Bond Defect (BD) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | + | 0 | 0 | 0 | 0 | + | + | 0 | + |
| | Die Shear Test (DST) | Defective Bond (DB) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | + | + |

## 4.0 Appendix

### Table I. Detailed Supporting Data

| | | | | | | |
|---|---|---|---|---|---|---|
| 5615* | 2N2946 | Q | 2D085 | WBT | WIRE BOND PULL TEST | UAI MARGINAL BOND PULL STRENGTH |
| 5856 | XR2207 | U | 3H210 | WBT | WIRE BOND TAIL TOO LONG | NON FLIGHT ONLY |
| [illegible] | [illegible] | U | 3J105 | WBT | BOND WIRES ON DIE | NON FLIGHT ONLY-DIE SURFACE IS PASSIVATED |
| 6092 | 26C32 | U | 3E134 | SEM | METALLIZATION VOIDS | UAI SPECIAL LIFE TEST SHOWS LOT OK |
| 5601 | FR19130 | Q | 4A124 | SEM | METALLIZATION | UAI MINOR DEFECT |
| 5950 | 54HCS02 | U | 1GG86 | SEM | METALLIZATION BRIDGE | UAI GATE ARRAY TECH. - DEFECT IN UNUSED AREA |
| 6013 | 2N2907A | Q | 4E035 | SEM | METAL LINES <30% | UAI CURRENT DENSITY CALC. OK FOR RPWS ONLY |
| 5988* | 26C32 | U | 2H225 | SEM | METALLIZATION VOIDS | UAI CURRENT DENSITY CALC. OK FOR APPLICATION |
| 6167 | 7533 | U | 3L030 | SEM | METALLIZATION VOIDS | UAI CURRENT DENSITY CALC. OK FOR APPLICATION |
| 4414 | 2N2905A | Q | 1GF64 | SEM | SMALL METALLIZATION CRACKS | UAI CURRENT DENSITY CALC. OK |
| 5873 | 2N5116 | Q | 2J027 | SEM | METALLIZATION LESS THAN 50% | UAI CURRENT DENSITY CALC. OK |
| 5442 | IRHF7230 | Q | 1H047 | SEM | SMALL METTALLIZATION CRACKS | UAI CURRENT DENSITY CALC. OK |
| 5613 | AD585S | U | 3J099 | SEM | SURFACE ANOMOLIES | UAI ANALYSIS SHOWS LOW RISK |
| 6088 | SPD5822 | D | 3G290 | SEM | DIE CHIPPED- RANDOM ANOMALY | UAI 5 MORE DPAs - ALL OK |
| 5908 | 2N2222A | Q | 2H055 | SEM | METAL THINNING TO < 50% | RTV |
| 5979 | 54HCS160 | U | 2E044 | SEM | VOIDS IN THE METALLIZATION | RTV |
| 5990* | 54HCSKMSR | U | 4F260 | SEM | CONTAMINATION | RTV |
| 6102 | 54HCS14KMSR | U | 5H143 | SEM | METALLIZATION DEFECTS | RTV |
| 6377* | 6617 | U | 2L016 | SEM | METAL THINNING TO < 50% | PENDING $ FOR FURTHER ANALYSIS |
| 6210 | CWR09 | C | 1A105 | SEM | DIELECTRIC VOIDS | NON FLIGHT ONLY |
| 5893 | 1N4569A | D | 4C211 | SEM | RADIAL CRACKS IN GLASS BODY | NON FLIGHT ONLY |
| 6272 | 2N2990 | Q | 4K021 | SEM | DIE CONTAMINATION | NON FLIGHT ONLY |
| 6612 | 54HCS02KMSR | U | 4C315 | SEM | METALIZATION VOIDS > 50% | NON FLIGHT ONLY |
| 6177 | HS1840 | U | 1C114 | SEM | METAL THINNING TO< 30% | NON FLIGHT ONLY |
| 5573 | 54HCS14KMSR | U | 4K050 | SEM | METALLIZATION DEFECTS | NON FLIGHT ONLY |
| [illegible] | [illegible] | D | 4C211 | SEM | CRACKS IN LEAD SEALS | FOR QCI TESTING ONLY IN UP-SCREEN |
| 5652 | D0N688 | D | 1J090 | RGA | WATER CONTENT TOO HIGH | UAI LIFE TEST PARTS OK |
| 5661 | D1777A | D | 1J089 | RGA | H2O EXCESSIVE | UAI ACCELERATED LIFE TEST OK |
| 5409 | 2N3501 | Q | 1GF68 | RGA | H2O EXCESSIVE | UAI TESTED 4 MORE, ALL OK |
| 5761 | 2N6137 | Q | 2C056 | RGA | H2O EXCESSIVE | UAI ANALYSIS SHOWS NO RELIABILITY RISK |
| 5925 | 10525 | U | 3F208 | RGA | H2O EXCESSIVE | UAI ANALYSIS SHOWS LOW RISK |
| [illegible] | [illegible] | Y | 2J018 | RGA | H2O EXCESSIVE AND BOND PULL | UAI ANALYSIS SHOWS RGA OK - BOND PULL OK |
| 5616 | 4N49 | B | 3H039 | RE | X-RAY-FOREIGN MATERIAL (BOND WIRE) | UAI ENTIRE LOT X-RAYED - PASSED |
| [illegible] | [illegible] | [illegible] | [illegible] | RE | X-RAY | NON FLIGHT ONLY |
| 5903 | 4N49 | B | 3H093 | LPIV | LOOSE WIRE INSIDE | UAI 4 MORE PARTS DPA - ALL OK |
| 6106 | 2N3375 | Q | 3D076 | LPIV | BOND WIRE ON DIE SURFACE | UAI SCREENING DATA OK - AREA PASSIVATED |
| 6190 | MA31750 | U | 2K070 | LPIV | VISUAL INTERNAL | UAI CURRENT DENSITY CALC. OK FOR APPLICATI( |
| [illegible] | [illegible] | [illegible] | [illegible] | LPIV | BOND WIRE SPACING TOO CLOSE | UAI 1 PART REJECTED - REST OF LOT OK |
| 5783 | 1047B | U | N1964 | HPIV | VISUAL INTERNAL | UP SCREENED AND USED |
| 5790 | 54HCS08 | U | 3H423 | HPIV | METALLIZATION VOIDS | UAI REDUCED CURRENT OK IN APPLICATION |
| 5993 | 1N 647 | D | 4B016 | HPIV | VISUAL INTERNAL | UAI LEAD PULL TEST ALL OK |
| 6617 | 54HCS02 | U | 4C315 | HPIV | METAL THINNING TO < 50% | RTV |
| 6282 | M39010/03A102KR | L | 9528 | HPIV | WIRE WOUND TOO TIGHT | PENDING |
| 6166 | 05041C332JA19 | C | 9331 | HPIV | CHIP CAP - COVER PLATE THIN | NOT USED |
| [illegible] | [illegible] | C | 9332 | HPIV | CHIP CAP - DIELECTRIC VOIDS | NOT USED |
| 6618 | 96J103 | Q | 2A072 | HERM | FINE LEAK TEST, WIRE BOND SUSPECT | UAI RGA OK FOR LARGE CAN - BOND PULL OK |
| 6619 | 2N2880 | Q | 1H036 | HERM | FINE LEAK TEST THREE TIMES | UAI PASSED RGA -MRB REVIEW APPROVED USE |
| 5513 | STD3303 | Q | 1H037 | HERM | FINE LEAK TEST | UAI PASSED RGA -MRB REVIEW APPROVED USE |
| 5644* | 2N2219A | Q | 1GF62 | HERM | GROSS LEAK TEST-ONLY DPA PART | UAI ENTIRE LOT PASSED LEAK TESTS |
| 5567 | IRM101W | U | 1C027 | HERM | GROSS LEAK TEST | UAI ENTIRE LOT PASSED LEAK TEST |
| 5568* | IRH190AH | U | 1C024 | HERM | FINE LEAK TEST | UAI ENTIRE LOT PASSED |
| 5494 | HN-1727 | I | 9524 | HERM | GROSS LEAK | PENDING |
| 5498 | HN1726 | I | 9524 | HERM | GROSS LEAK | PENDING |
| [illegible] | [illegible] | [illegible] | [illegible] | [illegible] | [illegible] | NOT USED |

| | | | | | | |
|---|---|---|---|---|---|---|
| 6157 | 1N4569A | D | 4B071 | EVI | LEAD SEAL LOOKS DEFECTIVE | JP SCREENED - 100% VISUAL AND LEAK TEST |
| 5431 | 1852 | X | 2)014 | EVI | GLASS SEALS HAD RADIAL CRACKS | JAI RADIAL CRACKS IN LEAD SEALS CHECK OK |
| 5992 | 422K | K | .71(025 | EVI | LEAD BROKEN | JAIE XTENSIVE ANALYSIS CONCLUDED LOW RISK |
| 5997 | TIL 24 | B | C1425 | EVI | PACKAGE DAMAGE | NOT USED |
| 6001* | CWR11 | C | 1C035 | EVI | PACKAGE CRACKS | NON FLIGHT ONLY |
| 6139 | 1N4848 | D | 3J131 | EVI | LEAD SEAL LOOKS DEFECTIVE | PARTS SCRAPPED DUE TO 100% VISUAL |
| 5879 | 1N6313 | D | 3C002 | DST | POOR DIE BOND | NON FLIGHT ONLY |
| 5858 | [illegible]757 | U | 9329 | DST | DIE & CHIP CAPACITANCE FAILS | NOT USED |

**Additional** detail:

| | | | | | |
|---|---|---|---|---|---|
| 6377 | AD585S | U | 3I099 | | 011 SURFACE WAS IRREGULAR ON 1 WO PARTS OUT OF THREE ALSO ON ONE VOIDS WERE S1 EN IN THE INSULATING OXIDE UNDER A BOND PAr) REDUCING THE THICKNESS 100.7" MICRONS THE SE PARTS HAD PASSED A 2(00 HOUR LIFE 11$1 AND THE MRB RF VIEW RESULTED IN UAI |
| 5988 | 11.1<913(I | Q | 4A124 | | 0 N). OF 1 w() PARTS SHOWED DAMAGED METALLIZATION (K TWO CONTACT WINDOWS TWO MORE PARIS FROM 1 HE SAME LOT PASSE r) DPA MRB ACTION WAS 70 UAI |
| 6001 | 422K | K | 3B025 | | ONE OF 11[1 LEADS WAS MISSING THIS LEAD TO AN EXTENSIVE ANALYSIS SINCE IN ASSEMBLY AI L or( AITV'()01111.R LEADS FRACTURED 1 HE CONCLUSION WAS THAT THE FRACTURES WERE CAUSED BY HYDROGEN EMBRITTLEMENT .1 III MRB DECIDED 1 HAT THAT AL 1 THE LEADS THAT WOULD FRACTURE HAVE ALREADY DONE s(1 DUE TO LEAD FORMING AND HANDLING NO RETROFIT WAS DONE |
| 5990 | 7573 | U | 3L030 | | S[ M EXAM FOUND THE METAL AI THE CONTACT WINDOW WAS REDUCED TO 35% 01 THE ORIGINAL THICKNESS CURRENT DENSITY CALCULATIONS SHOWED THE MET AI WAS ADEQUATE FOR TIJf APPLICATION MRB ACTION WAS 1(1 UAI |
| .s644 | 96J103 | Q | 2A072 | | THE LEAK TEST FAILURE WAS ATTRIBUTED TO A SURFACE FEATURE RF TESTING SHOWED NO LEAKS. THE BOND PULL FAILURE WAS AT145 GRAMS FORCE(gf) AND SHOULD BE 200gf. MRB REQUIRED THREE MORE PARTS 70 BE SUBJECTED TO BOND PULL TESTS AI L BONDS PASSED. MRB DISPOSITIONED I 01 UAI |
| 5615 | 2N2946 | Q | 2D085 | | ONE WIRE BOND OUT OF NINE FAILED THE PULL TEST IT ME ASURED 1 4gf AND SHOULD HAVE BEEN 1.5gf AT A MINIMUM 1 HE RE MAINING EIGHT BONDS PULLE r) AI 4.6 gf AS A MINIMUM MRff ACTION WAS TO UAI |
| 5568 | STD3303 | Q | II037 | | THE FINE LEAK WAS DETERMINED TO BE CAUSE r) BY SURFACE FEATURES |

Acronyms:
Log # = JPL FA 1.ab tracking number
Part # = JPL Generic part number
Trace # = JPL Lot tracking number
Test/Process Performed
- WBT = Wire Bond pull Test
- SEM = Scanning Electron Microscope Examination
- RGA = Residual Gas Analysis of the package cavity
- RE = Radiographic Examination (X-Ray)
- LPIV = Low Power Internal Visual Examination
- HPIV = High Power Internal Visual Examination
- Herm = Hermeticity Test
- EVI = External Visual inspection
- DST = Die Shear Test (attachment)

MRB = Material Review Board
UAI = Use As Is

[redacted]

# 10. Quality Assurance Site Survey Requirement

## 1.0 objectives

The objective of a Site Survey is to verify that the manufacturer uses standard, good manufacturing, test and handling practices, and is capable of building and delivering the product as specified. Findings likely to significantly impact reliability, cost, or schedule are documented and addressed in the survey,

## 2.0 Typical Requirement

1S0 **9001** paragraph 4.6.2 requires evaluation and selection of subcontractors on the basis of their ability to meet subcontract requirements. Although vendor qualification is required by NASA 1 Handbook 5300.4 (1 B) (1 B500) and our contract with NASA, in general JPL survey findings are generic industry issues which could drive reliability, cost or schedule, A survey is generally required every two years when procuring a spacecraft, subsystem, assembly (unit) or complex component from a vendor.

A survey consists of onc to five persons visiting a plant from one to five days depending on the complexit y of the manufacturing (component to spacecraft levels). A typical survey team consists of 2-3 persons including Quality Assurance (QA), and a packaging, fabrication, electronics or component specialist. A well organized survey team will meet prior to the survey to discuss the product and identify critical processes which should bc scrutinized during the survey,

Follow up audit(s) may bc required to verify that corrective actions have been properl y implemented; these audits are often combined with other business at the vendor.

## 2.1 **Rationale**

Vendors who arc new to military/space may not have the personnel, systems and/or equipment in place to build reliable flight hardware.

Vendors who have ncw management, have moved, or have lost key personnel sometimes "1osc the recipe" for building flight hardware. They may have made changes affecting the reliability of flight hardware manufactured in their plant.

Important areas which arc covered, if applicable, during a survey include:

1. contractor's Quality System
2. QA involvement in planning and reviews
3. Electro Static Discharge. (ESD) controls
4. Alerts
5. Procurement controls
6. Subcontracted manufacturing/testing operations
7. Approval, surveillance and auditing of subcontractors
8. Flow down of requirements to subcontractors
9. Non-standard parts approval and processing
10. Materials and parts qualification
11. Workmanship standards
12. Processes or tests new to the contractor
13. Process controls including those for unique processes or testing
14. Configuration management
15. Non-conforming Material Controls/Material Review Board

16. Material traceability
17. Receiving inspection
18. Manufacturing and test documentation
19. Rework/Repair
20. Statistical process control
21. in-process and Final inspections
22. End Item Data Package review
23. Packaging/Shipping
24. Document/Software change control
25. Self-audit program
26. C3canlincss/clean room controls/environmental controls
27. Test controls
28. Stamp control
29. Metrology controls
30, Training

Surveys can indicate a contractor's weakest processes or systems. This helps focus JPL's efforts to select the cent ract or, and plan oversight of the contractor's activity. For example, if a contractor had never before performed centrifuge testing, it would be prudent to review their centrifuge procedure in depth and require their QA to monitor or witness the test.

### 2.1.1 Avoidable Deficiencies/l~ailures

Listed are a few of the avoidable problems which may be identified during a survey:

1. Inadequate testing, products which do not meet the requirements of the contract, and/or hardware failures can result when requirements arc not adequately flowed down to subcontract ors. Manufacturers Sometimes contract out manufacturing or testing without sufficiently handing down customer requirements and maintaining controls over their subcontractors.
2. Hardware failure and/or loss of configuration management can result when engineering changes arc not communicated to the manufacturing floor duc to inadequate document change control.
3. Poor Electro Static Discharge control procedures can lead to functional or latent failures of hardware. "At JPL, over a two year reporting period ('91 -'92), approximately 30% of all electronic part failures that had failure analysis performed were attributed to ESD" (Ref. 2). These arc only the failures found after assembly.
4. New processes may introduce ncw failure modes. This will be dealt with during PDR/CDR if one is planned. 1 f not, the survey combined with manufacturing process review (see Process Review Requirement) maybe able to point out potential problems.
5. Vendors may say and believe that their standard processes meet contract requirements while a closer look may reveal that they do not.
6. Reliability of the hardware can be affected by processes and workmanship which tend to drift over time without recurrent training.

All of these problems, if experienced, are 1 ikel y to impact cost and schedule.

### 2.1.2 Supporting Data

Table 1 provides a sampling of problems detected during site surveys on JPL programs.

## 'J'able 1. JPL Site Surveys - Problems Encountered

| S/C | Survey Issues | Corrective Action(s) / Outcomes | Survey |
|---|---|---|---|
| - Spacecraft Solar Array | Contractor subcontracted a major portion of solar Array Drive Assembly and refused to do source inspection. | JPL did source inspection at subcontractor. Seven assemblies were built before onc passed shake test. The subcontractor dropped the flight solar Array Drive Assembly costing 6mos. delay & tens of thousands of $s. Unit failed 5 times in environmental test chrc to machined particles from grinding, operation. Several redesigns occurred duc to failures. | 039 |
| DOD Pathfinder (1986) Spacecraft | Approved. Follow up audits 10 survey revealed that contractor handed off cryogenic cooler to a subcontractor who contracted out the motor to the cryogenic cooler to another subcontractor with none of the project test requirements imposed on them It was a commercial motor. | JPL became heavily involved 2-3 trips/week thru delivery. JPL imposed space level testing on motor. JPL had sub-contractor disassemble & reassemble off the shelf motor so JPL would know materials & how it worked. Investigation spawned concern that motor brushes' life was not as long as the life of the mission. | 020 |
| NSCAT Crystcd oscillator | Loss of key personnel/facilities moved/management change. No operator/inspector training, Weak traveler design, No record of burn-in circuit tests prior to testing flight parts. | Disapproved but contractor was single source with unique capabilities. JPL became heavily involved - did some of the soldering Parts ended up working well. | 125 |
| Cassini Power Ssys SSPS hybrid | Contractor did not understand element evaluation and upscreening requirements, had never qualified a flight hybrid before, and had never purchased ASICS for use in flight hybrids. | J}'L. became heavily involved in this procurement. Parts are presently working well. | 146 |
| Cassini Waveguide | Approved. Post award survey. Previous experience on NSCAT had revealed: Contractor herd neither tools nor expertise to measure sophisticated waveguide geometry and stacked tolerances. Parts shipped to JPL did not meet drawing dimensions. Delays of several months and additional JPL trips to bring equipment and instruct contractor on its usc ensued. | Sur vey recommended contractor purchase appropriate equipment. Contractor purchased measuring equipment. No significant problems experienced to date. | 282 |
| Cassini Solid State Computer | Disconnect between computer assembly facility and parts acquisition group, Limited flow down of parts requirements, change nolices/corrective actions/MRB decisions. Loss of key person-no data review of parts. ESD controls not uniformly enforced. Limited QA involvement. | JPL QA resident heavily involved. Parts were marked on wrong side & assembled marked side down duc to disconnect between assembly & parts facilities- loss of serial number level traceability. | 210 |
| Cassini Print-cd Wiring Boards | Conditionally approved. Contractor had moved. Equipment out of calibration, DESC certification had not been renewed since move. | Corrective actions: Vendor to complete recertification. Equipment to bc calibrated. Procedures to bc updated. | 120 |
| All Project s fasteners/ rivets/ drills | Not recommended. Contractor produces mainly commercial grade hardware. | Contractor not used for J PI flight procurements. | 206—" |
| All Projects locking fasteners | Conditionally approved. Raw material control is not implemented. Quality Manual dots not address raw material traceability. | Recommendations: Implement raw material control. Quality manual should reflect traceability requirements. | 259 |
| - Engine Gimbal Actuator Bearings | Conditionally approved. Problem with traceability of raw material to heat number/manufacturer. Possible GIDEP Problem Advisory re: wrong materials used on bearings. | GIDEP Problem Advisory for warded to contractor. | 258 |
| Cassini electronic parts testing | Conditionally approved. Vendor has onty 6 months experience with class "S" flow & QA does not actively follow that flow for their single class "S" customer (customer QA monitors flow) | | 132 |
| Cassini A-D Converters/ hybrids | Conditionally approved. Verification of released test software is lax - danger that current version is not in use. Element evaluation and housekeeping issues aiso cited. | Frequent J PI QA and engineering trips at added cost. Parts arc currently working well. | 179 |
| Pathfinder DC-DC converter hybrids | Post-Award Survey. Process controls inadequate. Process logs and tables referenced in process documents were not found on production floor. No cleanliness monitoring. Poor production practices. No evidence of calibration of critical equipment. No document change control for test procedures. ESD controls arc weak. | Contract was placed because pr icc was low and schedule tight. Some parts failed electrically due to workmanship. Destructive Physical Analyses (DPAs) failed. Extra JPL trips duc to problems. Pam pawed qualification & are working. | NR |
| Cassini electronic parts testing | Conditionally approved. Non-responsiveness to prior JPL corrective action (CA). Rough handling of parts. | Corrective actions recommended: Respond to CA. Operator orientation/QA surveillance of parts during test. Increase staffing to accommodate workload | 105 |
| Cassini TWTA | Conditionally approved. Subsequent weakness m Quality engineering involvement, test coverage and end-item data submittal. | Significant JPL Quality Engineering involvement - limited improvement in supplier QA role. | 292 |
| Galileo AACS | ESD controls/procedure lacking. Contractor insensible to easily damaged (at 30 volts) integrated circuits. | J})l. negotiated stringent ESD procedure. JPL QA resident required to monitor ESD practices. Supplier improved - few problems on Magellan and Cassini. | NA |
| Galileo" Power Ssys Relays | Post-award survey disclosed material / configuration / process controls not well planned nor documented. | Significant JPL QA resident role. Delayed production as material and process problems surfaced. Eventually resolved - few problems on subsequent Cassini procurement. | NA |

**Survey = Quality Assurance Survey** number NR= Informal survey - not released NA= Survey not available

## 3.0 Tradeoffs

The survey tradeoff considers the cost of performing the survey and following up on correct ive actions versus a reduction in expected failures, cost and schedule overruns duc to poor quality hardware.

Pre-Award Surveys have the greatest potential for cost and schedule savings in that JPL has timely opportunit y to negotiate corrections or take an alternate approach to the procurement, Cost savings can also be expected when a better vendor is selected.

Pre-Award Surveys for fixed price contracts offer opportunities to contain cost within the contract and identify hidden costs of JPL contract oversight.

## 4.0 References


1. NHB 5300.4(111), "Quality Program Provisions for Aeronautical and Space System Contractors", NASA Handbook, April, 1969.
2. Olsen, "Electrostatic Discharge (ESD) Control Program Requirement", April, 1996.
3. QAP 39.3 Rev.D, "Survey of Quality Assurance Systems and Facilities Flight Systems Contractors", JPL Quality Assurance Procedure, July, 1992.
4. QAP 41.20, "Survey of Flight Electronic Microcircuit Parts Suppliers", JPL Quality Assurance Procedure.
5. QAP **41.21,** "Survey of Flight Electronic Part screening Contractors", JPL Quality Assurance Procedure.
6. QAP 41.22, "Survey of Flight Microelectronic Hybrid Manufacturers", JPL Quality Assurance Procedure.
7. QAP 41.23, "Survey of Flight Electromagnetic Suppliers", JPL Quality Assurance Procedure.
8. QAP 41.24, "Survey of Flight Semiconductor and Discrete IC Part Suppliers", JPL Quality Assurance procedure.


## 6.0 Acknowledgment


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# 11. Electrostatic Discharge Control Program Requirement

## 1.0 Objective

Electrostatic discharge (ESD) control requirements are used to protect electronic parts and systems against damage or degradation from ESD during routine handling, fabrication, testing and USC. The objective of an ESD control requirement is to ensure that electronic systems operate as intended during development, launch and mission operations.

## 2.0 Typical Requirement

Proactive measures exist to protect ESD-sensitive (ESDS) parts and systems against the devastating effects of ESD. Several military and industry ESD control standards exist. JPL's ESD control program is defined in JPL D-1348, JPL Standard for ESD Control. in summary, this program contains requirements including:

1. Personnel ESD awareness and control training
2. Personnel grounding techniques
3. liSD-safe workstations and laboratories
4. I iSD-safe packaging
5. ESD control facility audits
6. I;SD-safe handling procedures
7. I ;SD-protective clothing
8. Control of relative humidity levels

## 2.1 Rationale

The rationale for an ESD control program is based on the fact that ESD can severely damage or degrade electronic parts and systems. Industry estimates are that ESD accounts for 10SSCS over $1 billion in the US each year. At JPL, over a two year reporting period ('91 -'92), approximately 30% of all electronic part failures that had failure analysis performed were attributed to ESD.

ESD-sensitive electronic parts include discrete devices such as diodes, transistors, thin film resistors, charge coupled devices, surface acoustic wave devices, optoelectronic devices, hybrid integrated circuits, silicon controlled rectifiers, oscillators, microwave solid state devices, and integrated circuits. Integrated circuits are particularly vulnerable to ESD because of the small size of the constituent elements and their low thermal mass and low breakdown voltage. ESD will continue to be a problem affecting electronic parts, Semiconductor technological advancements are making parts smaller, faster, more complex, and requiring less power. As a result, electronic parts arc becoming more susceptible to ESD.

By definition, ESD is the sudden transfer of electrical charge between two objects at different electrical charge potentials. Electrical charge, sometimes called static electricity, is a natural phenomena that occurs from routine handling, fabrication, testing and usc of electronic systems. One technique to generate static charge, the triboelectric method, occurs when two dissimilar materials contact and separate. The contact-separation process creates either an excess or deficiency of electrons on both objects. Since electrons exhibit a negative electrical charge; an object with an excess of electrons is said to be negatively charged. Likewise, an object with a deficiency of electrons is said to be positively charged.

Onc example of the contact-separation charging phenomena occurs when a person wearing shoes walks across carpet. The contact and separation between the carpet and the shoe SOIC causes charge separation within both surfaces. Opposite free charges within the persons' skin layer are

attracted to the charges at the sole-skin interface: The result is a charge imbalance on the surface. of their body. If the person contacted a conductive object such as a doorknob, free charges within the doorknob and the person would suddenly move. 'l'his sudden movement of charges is an ESD event.

Studies have shown that tribocharging of the human body in the manner described above can generate voltages in the 20,000V range. This voltage, if allowed to contact an HSD-sensitive electronic part or system could cause devastating internal damage, One method that is commonly used to reduce human body charges to safe levels is to electrically ground the person. Personnel grounding is routinely accomplished using a wrist strap, which allows neutralization of the body surface charges.

Charge can also be generated inductively. Inductive charging differs from trioboelectric charging since charge transfer occurs without physical contact. Inductive charging results when one object is placed within the invisible electric field of an electrically charged object. The charged object exerts a force on the object placed within its field, creating charge separation within the object. If the object were conductive and grounded while within the field, a net charge of opposite polarity would be transferred. An example of inductive charging occurs when an electronic part is placed near an electricall y charged object such as an insulator that has been tribocharged. 1 nternal part damage may be induced depending upon the strength of the electric field. Techniques have been developed to protect ESD-sensitive (13 DS) items from electric fields, One example is the use of enclosing ESDS parts within metal lized barrier bags which blocks the force and charging effect of the electric field.

If not cent rolled, ESD will induce damage within ESDS parts and systems, This damage may lead to cit her catastrophic failures (the part doesn 't work) , parametric failures (the part works, but not correctly), or it may remain latent (hidden) only to fail at some time in the future.

isolation and replacement of catastrophic and parametric failures is usual] y possible, since they are often revealed during product development stages. Replacement of latent failed parts may be possible depending upon the type of product. However, replacement of a latent failed part on the. majority of JPL products is currently impossible, since these products arc spacecraft. A latent part failure on a launched spacecraft could lead to reduction of mission objectives or possible loss of mission. Thus, the prime rationale for an ESD cent rol program requirement is to safel y protect liSD-sensitive parts and equipment against catastrophic, parametric and most importantly, latent part failures.

### 2.1.1 Failure Modes

Common ESD-induced failure modes are listed below. These modes are indicative of internal damage sufficient to cause either catastrophic or parametric fai lures. Latent damage is difficult, if not impossible to detect.

1. Open circuits.
2. Hard short circuits.
3. Resistive short circuits.
4, Leaky input/output current.
5, intermittent operation,
6. Unstable operation.
7. Functional failure.
8. Out of spcc failure.

Figures 1 and 2 show examples of ESD-induced damage within an integrated circuit,

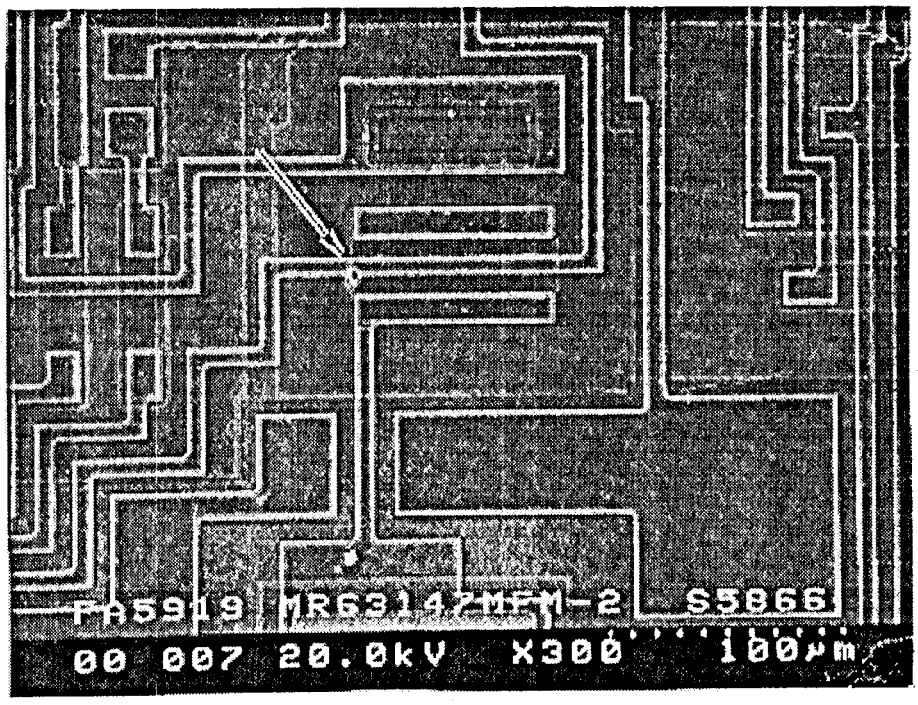



**Figure 1.** Scanning electron micrograph (x300) showing internal circuitry within an integrated circuit. Arrow denotes ESD-damaged location.

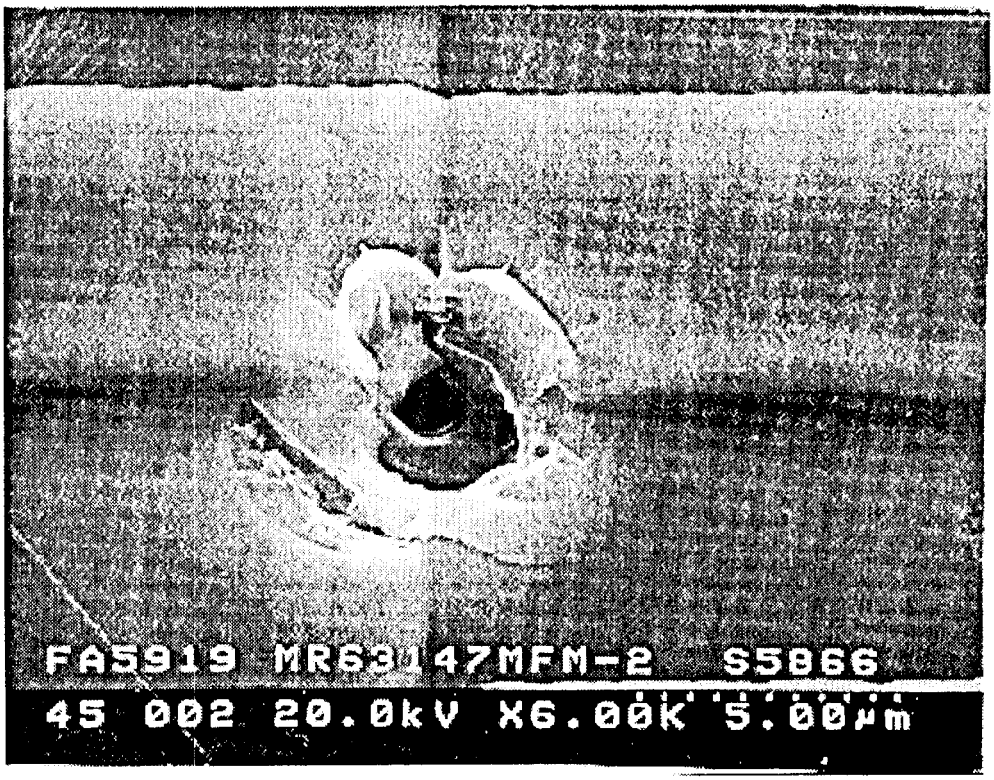



**Figure 2.** Scanning electron micrograph (x6000) showing close-up of ESD damage denoted by arrow in Figure 1.

### 2.1.2 Supporting Data

The JPL PFR database was searched for failures attributed to ESD. A partial list of ESD-induced failures are shown in Table 1.

**Table 1. Partial list of Problem/Failure History of ESD-related events**

| s/c | PFR # | Environment | Description | Failure Mode |
|---|---|---|---|---|
| Voyager | 39620 | Ambient | control logic #203 current high, bad IC U54 | ESD damaged CMOS IC |
| Galileo | 44101 | Ambient | CCD image sensor g100 no response (o light | ESD short caused by ESD. |
| Mars Pathfinder | D0850 | Ambient | When turning system on, the CCD did not deliver an image. | ESD damaged CCD |
| Ulysses | 3648 | Ambient | Phase multiplexer switch module inoperative | CMOS switch shorted due to ESD. |
| WFPC 1 | 53937 | Ambient | CCD failed to image properly. | ESD damage causing short in output gate region |
| Cassini | D0436 | Ambient | Gates of GaAs FETs were shorted | ESD damage |

## 3.0 Tradeoffs

The ESD control program tradeoff considers the cost of implementing the program versus the cost of incurring ground based (catastrophic and parametric) and flight (latent) failures. Ground based failures result in increased costs for troubleshooting, part isolation, part removal, and schedule slips. Relating a cost to latent failures is dependent upon the amount of mission objective lost and the monetary value of lost spacecraft science data.

## 4.0 References

1. JPL D-1348, Rev. B, JPL Standard for Electrostatic Discharge (ESD) Control, March 1996.

## 5.0 Bibliography

1. McAteer, Owen J. "Electrostatic Discharge Control", McGraw-Hill, New York, 1989.
2. Reliability Analysis Center, "Electrical Overstress/Electrostatic Discharge (EOS/ESD) Guidelines, Rome , New York, 1995.
3. American Society for Materials, " Microelectronic Failure Analysis" , Ohio, 1993.

# 12. Spacecraft Grounding Requirement

## 1.0 Objectives

The objective of grounding requirements is to have a grounding architecture that minimizes electrical noise and interference between the various electrical and electronic components of a spacecraft.

## 2.0 Typical Requirements

Electrical and electronic grounding of a spacecraft flight system must be coordinated by the system integrators. The system integrators must define an architecture (framework, plan, ground tree) that specifics the grounding paths and electrical isolation of power and signal interfaces. It is desirable to have a grounding system that prevents mission failure of a single short circuit failure of the power bus to chassis. The architecture must be clear and understandable, and verifiable by measurement. Each subsystem or other element must be designed to coordinate and be compatible with the system level grounding architecture. When buying off-the-shelf equipment, it may be appropriate to modify best practices if only minor performance degradation is expected. Whatever is used, there must be clear and complete documentation of the rules, and a separate explanation of why the final grounding architecture was selected.

The grounding requirements generated by the system integrators should include the following interfaces:

1. Single voltage power distribution or multiple voltages.
2. Power bus chassis isolation.
3. Power source isolation,
4. Power interface load isolation.
5. Signal, command, data, and telemetry interface isolation.
6. Attitude control interface isolation.
7. RF interfaces.
8. Pyro interface isolation.
9. Special interfaces.

Typical requirements are as follow. The bigger the satellite and the greater the cost and reliability needs, the more it should comply with the "best practices" identified in each paragraph.

Single or multiple voltage power distribution, Many spacecraft distribute a single voltage such as 28 volts, and the user loads provide isolation and power conversion as needed at the load. Best practice for larger spacecraft is to have the user loads isolated; this is implemented by a single voltage distribution, with isolation and power conversion supplied by the user load.

Power bus chassis isolation. Occasionally a spacecraft failure is attributed to a short circuit from the power bus high side to chassis. This can be eliminated by isolating the power system from chassis. Best practice for larger spacecraft is to have the power system isolated by some degree from the chassis. This deviates from common practice, where the battery on some common point is connected to chassis. Also, an isolated power bus may generate more radiated noise that could interfere with low frequency electric field measuring experiments on satellites.

Power source isolation. Isolation of the power source (solar array, battery, etc.) is a natural consequence of the spacecraft grounding architecture. The source should comply with the ground fault or other requirements of the spacecraft. Best practice is to keep the power source ungrounded, and have chassis grounding done at a separate well-defined location.

Power interface load isolation. User loads should comply with the system requirements. Best practice is to have user loads electrically isolated from the main power bus in the power converter. This prevents chassis ground loops (no uncontrolled power currents in the chassis). The user then provides chassis ground references for their internal secondary voltages.

Signal, command, data, and telemetry interface isolation. Signal electrical interfaces usually early a ground wire across the interface. Best practice is to DC isolate the interfaces from one subsystem to another to prevent ground loops. isolation of grounds is preferred.

Attitude control interface isolation. Attitude control subsystems are special in that their sub-elements are located in many places on a spacecraft. Also, they may be purchased from many vendors. Best practice is to keep their ground reference electricall y isolated from chassis at the sensor devices, and provide chassis ground reference at the attitude control central location.

RF interfaces. RF signals have capacitative coupling to ground. Best practice is to run such signals in coaxial cables, The coaxial cable shield is electrically attached to chassis at numerous points.

Pyro interface isolation. Pyro devices (squibs, electroexplosive devices) are operated by a large current (5-20 amperes) which has the possibility of coupling noise onto nearby victim devices. Pyro devices, during firing, can create a transient ground fault connection from the power firing lead to chassis due to the hot conductive plasma of the explosive charge. Best practice is to have the pyro firing unit electrically isolated from the power source, its signal and command interfaces, and from chassis. This will limit the firing current to be contained in the firing wires only.

Special interfaces. Special grounding requirements may be imposed by some users, especially science instruments. The system integrators must be sensitive to the needs of users. Coordinat ion at an early stage will permit inclusion of these special needs into the grounding architecture plan for a spacecraft.

Figures 1 a and 1 b illustrate best practices for all these concepts, and also illustrate a clear documentation of the "ground tree".

### 2.1 Rationale

The rationale for having knowledge and control of the spacecraft grounding is to reduce the likelihood of electromagnetic interference problems during operation, and to reduce the like] ihood of in-flight failures caused by possible ground fault modes.

#### 2.1.1 Relevant Failure Modes

Failure modes for ground faults include:

]. Power bus short circuits to chassis, with power loss or mission ]0ss.
2. Pyro firing fault currents to chassis, with resultant noise at victim devices.
3. "Ground loops" of current through chassis, with electrical noise and magnetic fields,

#### 2.1.2 Supporting Data

Supporting data may be found in JPL D-13427 (to be published), and is summarized in the following table of flight failure histories. Table 1 shows a history of spacecraft that support these recommendations.

**Table 1. System Grounding and Isolation Used in Various Spacecraft**

| Space-craft | Power System type/ voltage | Ground Type Power | isolation to Structure/ Resistance & Capacitance' | Ground Type, Signal | Ground Type, Pyro | Grounding Problems |
|---|---|---|---|---|---|---|
| Mariner-2 (1962) | Solar arrays/batt. 30 VDC; 50 V rms, 2.4 kHz AC | Rtn to Structure | N/A | Single ground reference with isolated IFs | Switched from battery | Short to Str, one solar array |
| Viking '75 Orbiter (1975) | Solar arrays/batt. 50 VAC; 30 VDC | Isolated from structure | AC 47 k ohm to str, each line; DC 3k ohm paralleled with 0.01 uF on return to structure | Single ground reference with isolated IFs | Isol. 5k ohm and 0.1 uF to Str. | Inverter failed at 1 ander release pyro event. |
| Voyager (197"7) | RTG 30 VDC; 50 V rms, 2.4 kHz AC | Balanced to structure | AC 47 k ohm & DC 10 k ohm symmetrically isolated & 0.1 uF DC return to structure | Single ground reference with isolated I/Fs | Isol. Sk ohm and 1uF to Str. | False telemetry readings at pyro fire: cause: 1 uF |
| Seasat (1978) | Solar arrays & battery | Isolated from structure | ? | SPG each assy; IFs not isolated | ? | Slip ring short hi to low may be fail cause at 6 months |
| Magellan (1989) | Solar arrays/batt. 28 VDC; 50 V rms, 2.4 kHz AC | Balanced to structure | AC 47 k ohm & DC 2 k ohm symmetrically isolated & 0.1 uF DC return to structure | Single ground reference with isolated I/Fs | Isol. Sk ohm and 0.1uF to Str. | Anomaly after SRM casing release pyro event |
| Galileo (1989) | RTG 30 VDC; 50 V rms, 2.4 kHz AC | Balanced to structure | AC 47 k ohm & DC 2 k ohm symmetrically isolated & O. 1uF 1 DC ret urn to structure | Single. ground reference with isolated I/Fs | 1s01. 5k ohm and O. 1uF to Str. | Slip ring leak, pwr to chassis. (acceptable) |
| Hubble (1 990) | Solar arrays & battery/ 28 VDC | SPG Rtn to structure | True star ground, " with very long wires | Multipoint; str. currents for signals | N/A (No pyro) | None (NOTE: very low ohms isolation) |
| Mars Observer (1992) | Solar arrays & battery / 28 VDC/10 VDC | Rtn to structure with 2 "SPG"s | N/A | Multipoint; Str currents for signals | Rtn to Str | 100% loss; cause unknown; during pyro event |
| TOPEX (1992) | Solar arrays & battery / 28 VDC | Rtn to structure | N/A | Single gnd rcf w/ isolated 1 Fs | Switched from battery | None |
| NOAA-13 (1 993) | Solar panels & battery | SPG Rtn to Structure | N/A | Multipoint; str. currents for signals | Rtn to Sir. | Hi-side short to Str 1 rno after launch. 1 00% loss |
| Cassini | RTG I 30 VDC | Balanced to structure | 2 k ohm each, high side and return to structure; 0.1 uF Rtn to Str . | Single ground reference with isolate.d I/Fs | Isol. Sk ohm DC & AC | sch. 1997 launch. Sec. Appendix A |

NOTES: Rtn: return; Str: structure; some cells may be left empty due to lack of applicability ("N/A") or lack of knowledge ("?")

## 3.0 Tradeoffs

Failure mode sensitivities and cost tradeoffs for the grounding design are illustrated in Table 11. The primary design variables are as listed in "design control parameters". Each design parameter may be a cost driver.

Table 11. **Control Parameter Sensitivity and Cost**

| Require-ment | Design Control Parameter | cost | Failure | Sensitivity to Use of Des. Ctl. Parameter | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| Electrical and electronic grounding | 1. single or many V. distribution | 0 | power high side short | N | Y | Y | Y | y | y | y | Y | Y |
| | 2. power bus chassis isolation | + | pyro fault current | N | N | N | N | N | N | N | Y | N |
| | 3. power source isolation | 0 | ground loop noise | Y | Y | Y | Y | Y | Y | N | Y | Y |
| | 4. power bus load isolation | + | ground loop dc msg. | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| | 5. signal interface isolation | + | | | | | | | | | | |
| | 6. attitude control IF isolation | + | | | | | | | | | | |
| | 7. RF interface isolation | 0 | | | | | | | | | | |
| | 8. pyro interface isolation | + | | | | | | | | | | |
| | 9. special interfaces | + | | | | | | | | | | |
| | | | | | | | | | | | | |
| | Cost: + = more to do; 0 = none | | Sensitivity Y means parameter controls failure Mode | | | | | | | | | |

## 4.0 References


1. "JPI, Spacecraft Electrical Grounding Architecture Design Guidelines," JPI. D- 13427 (to be published).

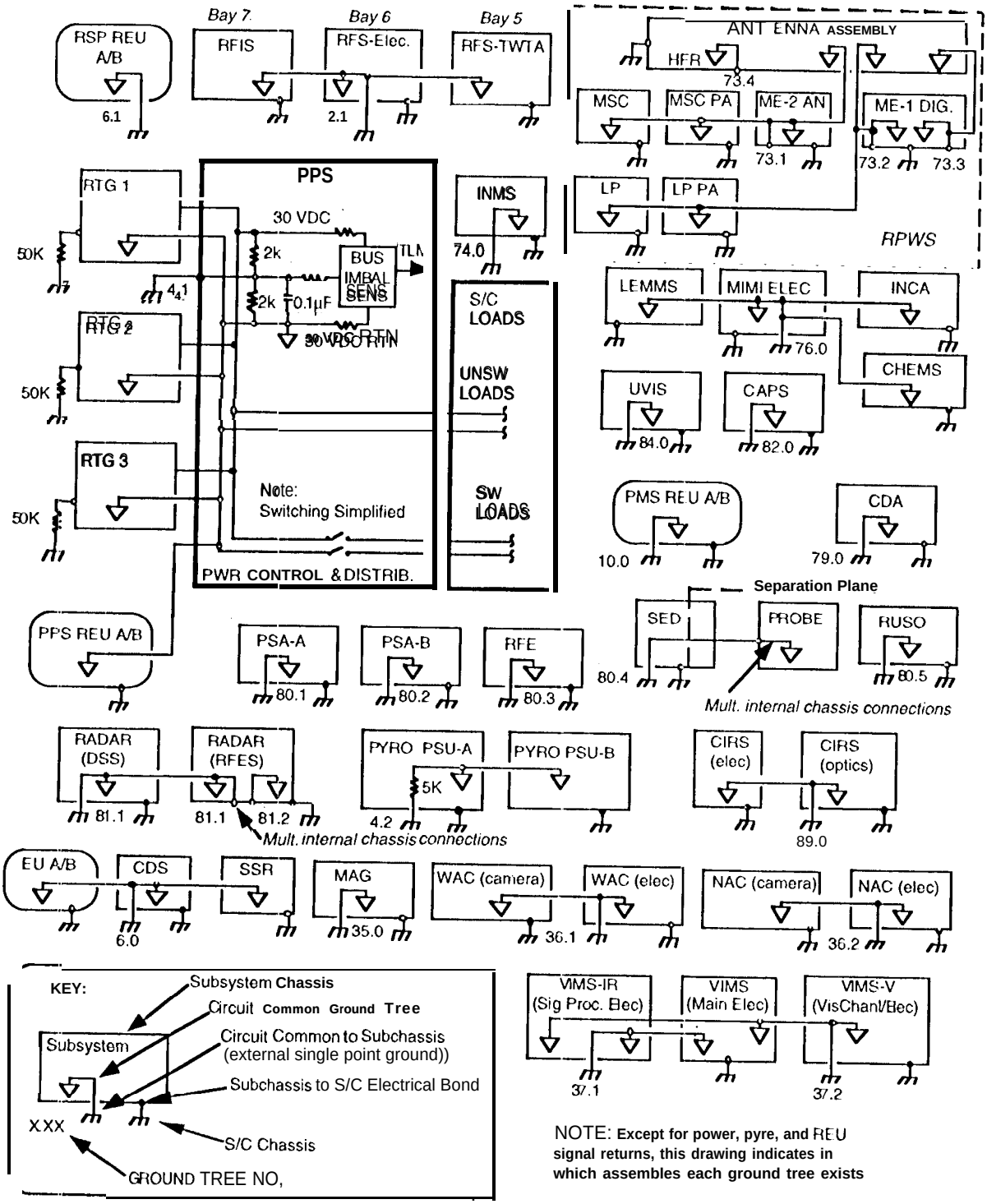
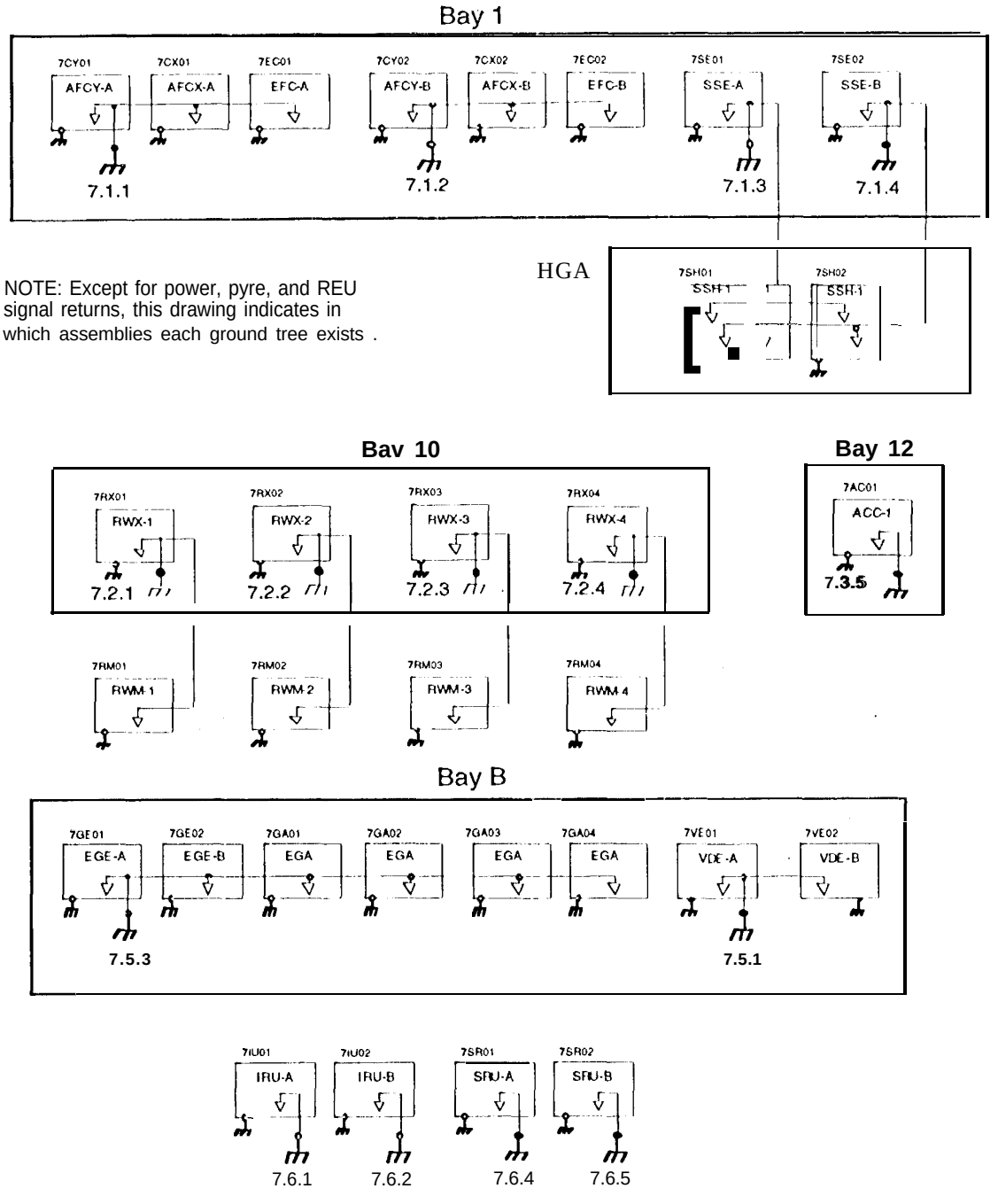



FIGURE **3-260:-02, CASSINI GROUND TREES,** Page 1 of **2**

3124195
(2189J)

Figure 1a. Illustration of Best Practices for Electrical Grounding and Documentation (1/2)




AACS Ground Trees

11/21194
(2189H)

Figure 1 b. Illustration of Best Practices for Electrical Grounding and Documentation (2/2)

# 13. Flight Electronic Parts QA Inspection Requirement

## 1.0 Objectives

Flight electronic parts quality assurance (QA) inspections include receiving, pre-screen, post-screen, and kitting inspections on flight parts.

The objective of performing receiving inspection on electronic parts is to screen out visual, dimensional, and pedigree rejects, particularly Iot-related rejects at the earliest possible time.. The objective of performing pre-screen inspection is to maintain traceability of serialized electronic parts, while the objective of performing post-screen inspections is to identify electronic parts damaged during screening (can be any kind of mechanical or electrical tests), as well as segregating screening rejects. The objective of performing electronic parts kitting inspection is to verify that the parts have successfully passed all of the required tests and inspections. Kitting inspection also verifies that the parts arc flight read y and that al i non-conformances have been properl y dispositioned.

## 2.0 Typical Requirements

1S() 9001 paragraph 4.10.2 requires a supplier to ensure that the incoming product conforms to specified requirements by means of inspection or other verification method,

NASA Handbook 5300.4( 1 B) paragraph 1 B705 requires inspection to verify compliance with purchase order or contract specifications. This inspection is performed cm procured articles prior to installation into the next higher assembly level. The inspection also includes records review.

Receiving inspection of electronic parts consists of
1. Visual inspection of 10070 of parts under magnification.
2. Verification that the parts are as specified on the purchase order or requisition,
3. Verification that the Certificate of Conformance is accurate.
4. Sample dimension inspection.
5. Verification of other pedigree requirements, as specified by the Parts Specialist on the Parts Pedigree Traveler (PPT). (Note: The Parts Specialist reviews Alerts applicable to the parts ordered when generating the PPT.)

Prc-screen inspection of parts going out for testing consists of
1, Cursory visual inspection,
2. Traceabilit y - recording serial numbers.

l'ost-screen inspection consists of
1. Visual inspection of 100% of parts under magnification.
2. Segregation of screened rejects.
3. Traceabilit y.

Kitting Inspection of electronic parts consists of:
1. Cursory visual inspection for handling damage.
2. Verification that all serial numbers are acceptable for flight, all discrepancies have been dispositioned, and all required tests and inspections have been completed.

## 2.1 Rationale

Receiving inspection of flight electronic components is the earliest point at which lot related defects can be identified if no source inspection was performed at the manufacturer. Problems with parts

should be identified as early as possible so remedial action (e.g. return parts, have a new lot produced, or rework/repair of parts) can be accomplished prior to start of assembly. This will minimize schedule and cost impacts to the Project or Experiment. Schedule and cost impacts for "difficult to procure" parts maybe great if defects are not identified before assembly.

Manufacturers or distributors of electronic parts typically do not accept parts for replacement more than 60 days after delivery. Parts arc often purchased months or years before being kitted to the }'reject or Experiment. Rejects discovered after that time might not be eligible to be exchanged for good parts.

Pre-Screen inspection helps maintain serial number level traceability of the parts by identifying which serial numbers go out for screening. When partial lots arc tested, maintaining this information is important for part configuration management .

Post-Screen inspection allows identification of parts which have been damaged during testing and handling, It also allows parts to be segregated from flight-ready parts in Project Stores until qual ification testing is completed and data is reviewed. The rejects can then be removed from the lot prior to the good parts being blue scaled and placed in Project Stores.

Kitting inspection is necessary to verify that the electronic parts have passed all testing and inspections required by the Part Pedigree Traveler (PPT) and that known Alert-suspect parts are not k itted to the user. The PPT is the menu of requirements for a lot of parts for a Project or Experiment. PPT requirements are defined by Electronic Parts Engineering, Section 507. Kitting inspection verifies that the parts being delivered to the Project or Experiment are indeed acceptable flight quality parts.

It is important to note that prior to May 26, 1994, visually good parts were blue sealed & placed in Project Stores. All parts were expected to have kitting inspection, so the configuration management aspects of the part, e.g. Qualification testing (QCI) completion, passing Destructive Physical Analysis (DPA), data review completion, and x-ray inspection completion, would be verified at that time. in effect, any part procured prior to June 1994, those with a trace number less than 4F001, may be blue sealed in Project Stores but may not bc complete] y fright worthy.

### 2,.1.1 Failure Modes

A sample of the type of defects which can bc identified by the four different inspections is listed below:

**Receiving inspection:**

**A.** Visual

1. Cracks in glass seals may cause loss of hermeticity which can lead to internal corrosion or performance degradation - can cat away at conductors inside parts, causing opens.
2. Cracked ceramic bodies - damaged internal components, loss of hermeticity which can lead to internal corrosion.
3. Damaged or bent leads - not able to solder, not able to assemble due to configuration .
4. Exposed metal plates on capacitors - easily shorted by small conductive particles.
5. Parts marked incorrectly or illegibly, loss of date code or serial number level traceability - can bc a problem later if lot-related or serial number specific defects are later discovered.
6. Flaking, blistering or damaged metal plating - allows further damage to part if corrosive agents e.g. salts or water arc available, introduces metal particles to assembly which can cause shorts, inability to solder.
7. Foreign material / contamination on the body of the part - if conductive, can cause shorts; if corrosive, can eat away at the metallization, introduce contamination to the assembly.

**B. Dimensional**

1. Out of tolerance dimensions - parts may not fit on boards or in assemblies.

**C. Pedigree**

1. Alert against a part - industry wide or JPL known problem with a manufacturer's part.
2. Wrong part / wrong value.
3. Pedigree problems - e.g. source inspection was required but not performed,
4. Missing/incorrect Certificate of conformance (C of C) - statement from manufacturer that parts were manufactured & tested as ordered.

Pre-Screen inspection;

1. Gross physical defects.
2. Traceability maintenance.

Post Screen inspection;

1. Visual defects - all those listed under Receiving inspection, especially :
   a. Cracked glass seals - common with glass diodes.
   b. Damaged/bent leads.

Kitting inspection:

1. Destructive Physical Analysis (DPA) failed or incomplete.
2. Data review incomplete.
3. Unscreening of parts e.g. x-ray, Particle impact Noise Detection (PIND) test, hermeticity life test, etc. not completed.
4. Electrical or mechanical rejects being kitted as flight.
5. Gross visual defects e.g. parts which have been in flight stores for 10 years or more and have corroded leads.
6. Waiver(s) incomplete/missing.
7. Wrong parts being kitted.
8. Wrong quantity of parts being kitted.
9. Wrong serial numbers being kitted - e.g. half the lot was tested, the other half was not, and it is being kitted.
10. Open non-conformances - liens against part which have not been dispositioned.

### 2.1.2 Supporting Data

As a result of the Receiving inspection process, see Table 1, approximately 5% of the lots inspected (excluding "capacitors and resistors) had anywhere from one part to the entire lot not used for flight.

As a result of the Pre-Screen inspection process, see Table 2, approximately 1 % of the lots inspected had anywhere from one part to the entire lot not used.

As a result of the Post-Screen inspection process, see Table 3, approximate y 12% of the lots inspected had anywhere from one part to the entire lot not used.

As a result of the Kitting inspection process, see Table 4, approximately 6% of kit line items were either not used at that time (returned to stores [RTS]), dispositioned Non-Flight, or received liens which were not dispositioned within two weeks. Liens not dispositioned within two weeks probably meant that some aspect of qualification of the parts, e.g. Qualification testing (QCI), Destructive Physical Analysis (DPA), or data review, was not complete at the time of kitting, putting the lot at risk for bad parts being kitted to the project.

## Table 1. JPL Flight Electronic Parts Receiving Inspection Defect Rates (All Projects) Jan '93 . May '96

| Part type | # Lots Inspected | # Lots Rejected * | % Rejctd Rcvng Inspection | Disposition of discrepant material: Use As Is | Acceptable ** | Scrap or Non-Flight (NFT) | Return to Vendor (RTV) | Open = Not Dispositioned | % of lots receiving inspected with some parts or entire lot not used: % Open | % Scrap, NFT or RTV |
|---|---|---|---|---|---|---|---|---|---|---|
| All except cap/resistr | 1075 | 121 | 11% | 50 | 14 | 4 5 | 4 | 8 | 1% | 5% |
| All Parts | 3335 | 180 | 5% | 62 | 28 | 64 | 18 | 8 | | 2 % |
| Capacitors | 470 | 28 | 6% | 2 | 10 | 8 | 8 | | | 3% |
| Crystals/ Oscillators | 28 | 12 | 43% | 7 | 1 | 3 | | 1 | 4% | 1 1 % |
| Diodes | 203 | 38 | 19% | 21 | 3 | 12 | 1 | 1 | | 6 % |
| - | 13 | 3 | 23% | | 1 | | | 2 | 15% | 0% |
| Electro-magnetics | 23 | 0 | 0% | | | | | | . | 0 % |
| Integrated Circuits | 601 | 52 | 9% | 21 | 7 | 17 | 3 | 4 | 1% | 3% |
| Opto-electronics | 12 | 3 | 25% | 1 | | 2 | | | . | 1 7 % |
| Relays | 40 | 5 | 13% | 1 | | 4 | | | . | 1 o % |
| Resistors | 1790 | 31 | 2% | 10 | 4 | 11 | 6 | | | 1% |
| R.F. & Microwave | 9 | 0 | 0% | | | | | | . | 0% |
| S-Wins | 8 | 0 | 0% | | | | | | | 0% |
| Transducr | 36 | 0 | 0% | | | | | | . | 0% |
| Transistors | 102 | 11 | 11% | 2 | 2 | 7 | | | . | 7% |
| JPL Spec Parts | 699 | 99 | 14% | 46 | 11 | 33 | 3 | 6 | 1% | 5% |
| Non-JPL Spec Parts | 2638 | 4 8 | 3% | 20 | 18 | 27 | 15 | 4 | | 2% |

*Lot may be rejected for one part or entire lot.

**Acceptable disposition means that rejection was cleared up prior to disposition (e.g. needs a waiver and waiver was obtained to close out discrepancy) or the condition was not technically a reject.

Note: Receiving and kitting inspection of standard resistors and capacitors for all projects was eliminated in May 1994 due to findings of low reject rates and low risk for elimination of those inspect ions.

## Table 2. JPL Flight Electronic Parts Pre-Screen inspection Defect Rates (All Projects) Jan '93 - May '96

| Part type | # Lots Inspected | # Lots Rejected * | % Reject Pre-Screen Inspct | Disposition of discrepant material: Use As Is | Acceptable ** | Scrap or Non-Flight | Return to Stores (RTS) | open = Not Dispositioned | % open | % of lots pre-screen inspected with some parts or entire lot not used: % Scrap, Non-Fit or RTS |
|---|---|---|---|---|---|---|---|---|---|---|
| All except cap/resistr | 243 | 6 | 2% | 2 | 2 | 1 | 2 | | · | 1% |
| All Parts | 328 | 6 | 2% | 2 | 2 | 1 | 2 | | · | 1% |
| Capacitors | 4 | 0 | 0% | | | | | | - | 0% |
| Diodes | 41 | 2 | s% | 1 | 1 | | | | · | 0% |
| Integrated Circuits | 161 | 3 | 2% | 1 | | | 2 | | · | 1% |
| Resistors | 81 | 0 | 0% | | | | | | · | 0% |
| 'i ors | 25 | 1 | 4% | | | 1 | | | · | 4% |
| Other | 16 | 0 | 0% | | | | | | · | 0% |
| | | | | | | | | | | |
| JPL Spec | 145 | 2 | 1% | | | | 2 | | · | 1% |
| Other Spec | 186 | 4 | 2% | 2 | 1 | 1 | | | | 0.5% |

## Table 3. JPL Flight Electronic Parts Post-Screen inspection Defect Rates (All Projects) Jan '93 - May '96

| Part type | # Lots Inspected | # Lots Rejected* | % RejectPost Screen Inspct | Disposition of discrepant material: Use As Is | Acceptable ** | Scrap or Non-Flight | Return to Vendor (RTV) | Open = Not Dispositioned | % Open | % of lots post-screen inspected with some parts or entire lot not Used: % Scrap, Non-Fit or RTV |
|---|---|---|---|---|---|---|---|---|---|---|
| All except cap/resistr | 315 | 51 | 16% | 11 | 1 | 38 | | 1 | | 12 % |
| All Parts | 400 | 65 | 16% | 12 | 3 | 48 | | 2 | | 12% |
| Capacitors | 3 | 0 | 0% | | | | | | | 0% |
| Diodes | 60 | 15 | 25% | 2 | | 13 | | | · | 22% |
| Integrated Circuits | 183 | 18 | 10% | 8 | 1 | 8 | | 1 | | 4% |
| Resistors | 82 | 14 | 17% | 1 | 2 | 10 | | 1 | 18% | 12% |
| Transistors | 48 | 11 | 23% | 1 | | 10 | | | | 21% |
| Other | 24 | 7 | 29% | | | 7 | | | | 29% |
| | | | | | | | | | | |
| JPL Spec | 131 | 7 | 5% | 3 | 1 | 3 | | | - | 2% |
| Other Spec | 264 | 46 | 17% | 9 | 1 | 35 | | 1 | - | 13% |

Table **4 lists** defect rates at kitting inspection for specific part types. The final number to the right indicates the percentage of line items kitted which were rejected and either not issued to flight Projects or which were rejected and could not be used within 2 weeks of rejection.

'1'able 4. **JPL Flight Electronic Parts Kitting** inspection **Defect** Rates (All **Projects) July** '93 - **May '96**

| | | | | **Disposition of discrepant material:** | | | | | | | **% of kit line items not used** | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Part type** | **# Lots Inspected** | **# Lot Rejctd*** | **% Rejct Kit Inspection** | **Use As Is** | **Acceptable ** ** | **Scrap or Non-Flt (NFT)** | **Return to Stores - Kit not used** | Open = **Not Dispositioned** | **# Kits Open > 2 weeks** | **# Kits Open > 2 weeks or not used** | **% Kits Open > 2 Weeks** | **% Kits Open >2 weeks** or not used e.g. **RTS, Scrap, NFT** |
| All except cap/resistr | 2991 | 248 | **8%** | 20 | 142 | 9 | 37 | 40 | 167 | 192 | **6%** | **6%** |
| All Parts | 3348 | 257 | **8%** | 21 | 146 | 9 | 38 | 43 | 174 | I 99 | **5%** | **6%** |
| **Capacitors** | 58 * | 3 | **5%** | | | | | 3 | 3 | 3 | **5%** | 5 % |
| **Diodes** | 467 | 21 | 4% | 3 | 12 | | 2 | 4 | 16 | 18 | **3%** | **4%** |
| **Integrated** Circuits | **1974** | 189 | **10%** | **12** | **103** | **9** | 32 | 33 | **125** | 147 | 6 % | 7 % |
| **Resistors** | 299 * | 6 | 2% | **1** | **4** | | **1** | | 3 | **4** | **170** | **1%** |
| **Transistors** | 313 | **21** | **7%** | 3 | 15 | | 3 | | 12 | 13 | **4%** | **4 %** |
| **Other** | **237** | **17** | **790** | **2** | 12 | | | 3 | **14** | **14** | **6%** | **6%** |

*Kitting Inspection of standard capacitors and resistors was stopped for all Projects in May '94 due to low reject rates.

Table 5 provides a sample of problems detected during flight electronic parts receiving, Post-Screen and kitting inspections on JPL programs. This information is entered by Quality Assurance (506) into the Electronic Paris information Network System (EPINS) maintained by Electronic Parts Engineering (507),

## Table s. JPL Electronic Parts Receiving, Post-Screen and Kitting Inspection Defects

| Spacecraft | Part type | Type inspect n | Defect | Disposition / Outcome | Trace #, Date Code |
|---|---|---|---|---|---|
| Pathfinder | | kitting | Pathfinder did not fund JPL QA receiving inspection, kitting, inspection nor DPA. SeaWinds shared this lot of parts with Pathfinder. DPA was performed on parts for SeaWinds and failed duc to purple plague. Inspector noticed that same lot had been kitted to Pathfinder project Parts had already been kitted (without QA kit inspection) and assembled on boards. | Non-flight. Pathfinder was notified of problem. Another DPA of the lot was performed, the purple plague on these parts was worse than on the first DPA | 4H1058/ 9438; DPA Log # 6516; SEKLR # 57790 |
| Cassini AACS | IC | receiving | Qualification testing (life test, etc.) incomplete | UAI. Receive and kit parts prior to completion of QCI. | 2H101 I 9225 |
| Cassini CDS | IC | receiving | 22 parts lead damage. | Non-flight. | 1GG85 / 9310 |
| Cassini Mag | diode | receiving | Cracks in body of 90 diodes | Non-flight. | 3G084 / 9227 |
| MISR | diode | receiving | 12 parts cracked scat | Open | 3J004 J 9510 |
| Cassini CCCB | diode | post screen | 1 part body damage | scrap | 2K051/ 9326 |
| Cassini RFS | diode | post screen | 126 parts cracked bodies | Non-Flight | 3J131/ 9326 |
| MISR | resistor | post screen | 69 parts - marking error | UAI | 1}1086/ 9117 |
| Cassini AACS | IC | post screen | 6 parts lead damage | UAI | 0K026/ 9142 |
| C/C AACS | IC | receiving | Certificate of Conformance (C of C) from mfgr is incorrect. | [JAI | 4G026/ 9339 |
| Cassini AACS | IC | post screen | 3 parts-exposed base metal | Non-flight. | 4G026/ 9339 |
| SeaWinds CDS | IC | post screen | 13 parts-lid misalignment | UAI | 5J007/ 9442 |
| MESUR MR | xsistor | post screen | 12 miscellaneous | Non-flight. | 4D007/ 9412 |
| Cassini AACS | xsistor | post screen | 1 part - test incomplete | Non-flight. | 4C231/ 9303 |
| Cassini CCCB | xsistor | post screen | 1 part marking error | scrap. | I 1061/ 902 2 |
| MISR | diode | kitting | Pedigree/corrfrgcrration - DPA pending, data review incomplete, QCI incomplete. | DPA failed, dispositioned UAI 6 weeks later. Data review & QCI incomplete, dispositioned UAI. | 5A005 19520 |
| Cassini AACS | IC | kitting | Parts erroneously kitted without kitting inspection. Parts had not been screened; needed l) PA, Qual, and data review. | Project 10 return parts for screening. SEKLR # 63847. | 41'.260 / 934? |
| C/C Radar | | receiving | Dimensional - parts out of spec. | [JAI | 3G290/ 9315 |
| Sir-C | IC | receiving | Alert | Non-flight | 11011/8 931 |
| Cassini Radar | IC | receiving | 9 parts lead damage | Non-flight | 31101/9 41(I |
| MISR | diode | receiving | 6 parts marking error | Non-flight | 3K099/ 9341 |
| MISR | xsistor | receiving | 94 pm-s lead damage; 6 parts plating problem | Non-flight | 4A020/ 9446 |
| Cassini RFS | filter | receiving | 18 of 34 parts - void | OPEN | 4C281/ 9247 |
| Cassini CCCB | crystal oscilltr | kitting | 10 parts - data review incomplete. Open 8/25/94 till 3/14/9s, | Accept. Data reviewed & acceptable. | 2J019 / 9424 |
| MISR | switch | kitting | DPA pending. Open 9/20/95-12/14/95. | Accept. DPA completed. | 41060 / 940 I |
| Cassini 1SS | Optoele tronic | kitting | lest Incomplete. Open 6/14/94.9/20/94. | Accept. Test completed. | 31083 I 9413 |
| Cassini CCCB | xsistor | kitting | Waiver needed. Open 9127193- 101?7193 | Accept. Waiver obtained. | 2G001/ 9308 |
| Cassini RFS | xsistor | kitting | DPA pending. Open 5/4/94-5/16/94 | Return to Stores. | 3J076 / 9322 |

UAI=Use-as-is NI = Non-flight DPA=Destructive Physi l Analysis
QCI=Qualit y Conformance Inspection testing

## 3.0 Tradeoffs

The electronic part receiving inspection tradeoff considers the cost of performing the inspection and resolving non-conformances versus an increase in failures, cost, rework and schedule impacts due to defects which go undetected or are found at the board assembly or test level.

Receiving inspection of long lead-time, expensive, custom and hard to acquire items will enable Project or Experiment to receive the earliest notification possible if there is a problem. Early notification allows for a rebuild, if necessary. Timely notification also allows for return and replacement of defective parts; this might not be an option if defects are discovered at a later date.

Pre-Screen inspection is important to maintain serial number level traceability. Pre-Screen inspection has the least payoff for the effort (least bang for the buck) of all the inspections. If Project Stores would agree to identify which serial numbers go out for screening and provide that information to QA, then Pre-Screen inspection could be eliminated with minimal impact to quality or reliability.

The Post Screen inspection tradeoff considers the cost of performing the inspection and resolving non-conformances versus an increase in failures, cost, rework and schedule impacts due to defects which go undetected or are found at the board assembly or test level.

The kitting inspection tradeoff considers the cost of Electronic Parts Engineering preparing the Part Pedigree Traveler (PPT) and of QA performing the inspection and part configuration check, and resolving non-conformances versus an increase in failures, cost, rework and schedule impacts due to defects which go undetected or are found at the board assembly or test level. Kitting inspection should continue to be done. Kitting is the final check and the only gate to ensure all testing and inspection are complete prior to delivery to Project or Experiment.

The above tables contain data from parts procured primarily for Class A and Class B projects. These projects procured corresponding high grade parts. If more commercial and low grade parts are utilized in the future, the defect rates are expected to rise.

3.2 Sensitivities

**Table** 6. Control Parameter Sensitivity and Cost Sensitivity

| Requ' ment: | Control Parameters | FAILURE MODE | Sensitivity to Defect Detection + More Effective O Neutral - Less Effective | | | | | | | | cost |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | P | L | S | M | FM | D | GL | CP | CO | |
| | External Visual Inspection | Package (P) Leads (L) Seals (S) Marking (M) External Foreign Material (FM) Gross Leak (GL) | + | + | 0 | + | + | 0 | 0 | 0 | - | + |
| | Sample Dimensional Inspection | Dimensions /(Fit or Function) (D) | 0 | 0 | - | - | - | + | - | - | - | + |
| Receiving | Pedigree Check | Correct Part/Value (CP) Configuration/Certification (CO) | - | - | - | - | - | - | - | +- | + | + |
| Pre-Screen | Traceability Maintenance | Configuration/Certification (CO) | - | - | - | + | - | - | - | + | + | + |
| Post Screen | External Visual Inspection | Package (P) Leads (L) | + | + | 0 | + | + | - | 0 | - | - | + |
| Kitting | Cursory Visual Inspection | Package (P) Leads (L) | 0 | + | - | + | 0 | - | - | - | 0 | 0 |
| | Pedigree Check | Configuration/Certification (CO) | - | - | - | - | - | - | - | + | + | + |

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## 6.0 Acknowledgment


Jerry Berry, Wendy Ellery, Kathy Ellis, Robin Hill, and John Miller contributed to and/or reviewed this document.

# 14. Quality Assurance Plan Requirement

## 1.0 Objectives

A Quality Assurance Plan is the mutually agreed upon contract with project m" Experiment. It documents the planned level of quality assurance support, and how it would be implemented on the Project or Experiment.

## 2.(I Typical Requirements

1S09001 paragraph 4.2.1 requires suppliers to prepare a quality manual which covers the quality system of the supplier. in JPL's case, the amount and type of quality support varies depending on the risk level designated for a project and on the specific requirements of the project.

NASA Handbook 5300.4( 1 B) paragraph 1B206 requires the contractor to prepare, maintain, and implement a Quality Program Plan which serves as the master planning and cent rol document. The Quality Program Plan describes how the contractor would comply with quality requirements.

A Quality Assurance Plan is written at the beginning of the development phase of a Project or 1 :xperiment. It defines requirements to be implemented on a Project or Experiment, including:

1. Quality program management and planning (roles, responsibilities, authority and reporting).
2. Design and development controls.
3. Purchasing/procurement controls.
4. Quality requirements for subcontractors & suppliers.
5. Approval, surveillance and auditing of subcontractors.
6. Source evaluation,
7. Residency at major subcontractors.
8. Receiving inspection.
9. Inspect ion.
10. Planning.
11. Process controls (procedures and Assembly Inspection Data Sheets [AIDS]).
12. Workmanship standards.
13. Test surveillance: environmental and final acceptance.
14, Post test hardware inspection.
15. Control of non-conforming material.
16, Records and reporting,
17, Hardware reviews.
18, Spacecraft operations at JPL and launch site.
19. Handling, storage, packaging, preservation, and delivery/shipping controls.
20. QA verification of Safety requirements.
21, QA verification of Configuration Management controls.
22. Control of inspection, measuring and test equipment/ metrology controls.
23. Training and certification.

## 2.1 Rationale

in order to minimize risk, unforeseen cost incrcascs, and schedule slippage, it requires an up-front plan by Quality Assurance and Project or Experiment that specifics the mutually agreed upon qualit y requirements. 'I'he QA Plan states what and how it would be implemented. The QA plan gives ncccssary guidance to systcm engineers on hardware requirements. A released QA plan makes QA requirements readily available to Project personnel and provides a clear basis for planning purposes (Ref. 1).

Historically, flight projects have always had Quality Assurance Plans. QA Plans arc often written to a higher level than the acknowledged risk assigned to a Project. For example, a Class C project (as defined in D-1489) might have a class C+ or class B QA Plan. in these hybridized plans, the basic requirements of a class C project would be met and then selected requirements from class B or A projects are added to minimize risk of failures or schedule impacts.

### 2.1.1 Failure Modes

Listed below arc a few of the avoidable problems which a QA Plan addresses (Ref. 1):

1. Omissions and mistakes in planning QA operations.
2. Lack of visibility on QA costs.
3. Confusion among project personnel on QA requirements.
4. Unexpected requirements with hidden costs and schedule impacts.

## 3.0 Tradeoffs

The Quality Assurance Plan tradeoff considers the cost of implementing quality requirements versus increased risk of fai lure, schedule delays, and cost impacts to the Project or Experiment ,

## 4.0 References

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## 6.0 Acknowledgment

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# 15. Manufacturingg Process Review Requirement

## 1.0 Objectives

The objective of a Manufacturing Process Review is to identify any problems at the vendor that may pose a qualit y or reliabilit y risk for the project. Process review aims to proactively identify and control or prevent the use of new, unqualified, or uncontrolled processes on flight hardware.

## 2.0 Typical Requirements

1S0 9001 paragraph 4.9 requires contractors to control processes which directly affect quality.

NASA Handbook 5300.4(1 B) paragraph 1 B503 states that the contractor (JPL) shallconduct appropriate quality assurance activities to ensure that our contractors comply with applicable requirements.

Manufacturing Process Review takes place under the following circumstances:

1. Part of a facility survey or audit.
2. Project concerns - processes which arc new to the contractor, new to industry or have a history of problems.
3. Occurrence of a failure.
4. Inactive processes which are being reactivated.
5. Evidence that processes, procedures or equipment arc obsolete or out of control.
6. Potential for cost or schedule impacts.
7. Operators lack training or required Certifications.
8. Process experiencing excessive ]0ss or discrepancy rates.

Process review takes anywhere from one half day to a week depending on the complexity and number of the processes being reviewed. Typically a fabrication, process or packaging engineer from Quality Assurance or from another section at JPL performs the review. JPL personnel with several different areas of expertise may be required to review all processes.

For a survey related process review, the engineer typically skims the procedures used in building the device to identify critical processes or those with a history of problems.

For all reviews, the engineer looks at the complexity and maturity (revision history) of the processes. The reviewer will goes on the floor to observe the operators performing the process to sce if and how it is implemented, Review of written procedures may be done at JPL if the contractor allows copies of the written procedure to be removed from the premises.

Documents that may be reviewed include:

1. Procedures.
2. Material specifications.
3. Process specifications.
4. Traveler (process flow sheet) most closely resembling what will be built for JPL.
5. Materials and parts testing specifications.
6. Calibrat ion requirements.
7. Contamination and ESD control requirements.
8. Logs for such as ovens, freezers, bond pull test, die shear test, dye penetrant test.
9. Project or task specific documents and drawings.

The reviewer may: look at the machinery and overtemperature controls; inspect samples of items made by the contractor; observe how discrepant material is handled; examine the qualification status of equipment, personnel, facilities and materials; scc if the operators understand and operate to the current revision of the written documentation; and observe the operators working to the procedures, if possible. Basically, they want to sec that the contractor is doing what their procedures say they arc doing and that their procedures tell them to do the right thing.

## 2.1 Rationale

Process review allows for the inclusion of adequate controls and testing and for approval of materials. This helps to insure that reliable products which meet the JPL contract are delivered.

JPL often goes to Qualified Military Line (QML) or highly qualified contractors, and asks the contractor to disrupt their standard flow and do things they have never tried before. This is not bad, but it does invalidate their certification or qualification for those processes which do not follow the contractor's approved flow. Process review assures that those processes outside of the manufacturer's normal flow do not introduce unforeseen failure modes.

As onc of our process engineers wrote: "... wc are entering in an era where reduction in cost has driven JPL to enter into purchase agreements where manufacturers' procedures are being, utilized in place of JPI, procedures. We are finding a number of instances on Pathfinder . . . that the manufacturers do not have a standard procedure for building the parts which wc have requested and are developing new procedures as part of the contract. In addition, wc arc doing away with most on site inspections by JPL personnel." He recommended that J }'1. review production documentation and qualification of ncw processes prior to the manufacture of flight hardware (Ref. 1).

Contractors who are new to JPL should have their processes reviewed. Ncw or rc-activated processes of contractors familiar to JPI, should also be reviewed. Contractors who build JPL products on a QMI. or approved line may not need Manufacturing Process Review. Contractors **with** mature processes which have recently produced flight hardware for JPL projects with similar requirements also may not need this review. However, restart processes arc always troublesome. Ncw personnel, obsolete processes and methods, overage materials, and ncw or worn out equipment can nudge the process out of control.

Processes utilized on an ISO 9000 approved line may still need their critical processes reviewed. 1S0 9000 Certification only establishes that the vendor dots what they say they arc doing. It dots not say that they arc doing the right thing. 1S0 9000 surveyors can come from any industry (e.g. text iles) so may not be able to verify that contractor's processes arc appropriate for space.

### 2.1.1 Failure Modes

Some failure modes (not comprehensive) that timely process review can prevent include:

1. Appropriate cleaning steps included "on a traveler can preclude contamination, corrosion, poor solderability, poor bondability or poor scaling of surfaces.
2. Appropriate inspection steps included in the process flow can preclude catastrophic conditions from going undetected - defects that would not be inspectable after completion of assembly.
3. Appropriate choice of, certification of, and/or testing of materials (such as x-ray, dye penetrant, and ultrasonic) can preclude structural y weak or impure materials from being used.
4. Controls on the shelf life, mixing and handling of bonding materials can preclude poor adhesion.
5. Periodic testing and correction of chemicals in bathing solutions can preclude flaking or blistering of plating, poor welds, and poor solderability.
6. Proper weld schedules can preclude weak or fractured weld joints.

There are often several interrelated causes for a problem, Experienced evaluation is necessary to minimize the occurrences of problems, New processes commonly display new failure mechanisms.

### 2.1.2 Supporting Data

'1'able 1 provides a sampling of problems detected during manufacturing process reviews.

**Table** 1. Problems Encountered **During Manufacturing** Process **Review for Pathfinder and Cassini Projects.**

| Projec | Issue | Resolution/ Recommendation | Memo |
|---|---|---|---|
| Pathfinder Solid State Recorder | Part of SURVEY - Pick and place machine NEWLY MODIFIED try company held leads dcrwn during hot bar reflow, causing lead strain - latent failure mechanism | Contractor, when made aware by JPL of this, took machine off line & did not usc for J} 'l. procurements | FSQA 209-92 |
| Pathfinder Driver Modules | (1)Problem: Anomalous behavior of flight spares led to process review. After delid - large IC eutectic die attach material exhibited insufficient wetting. Die hrrd hccn bonded without scrubbing due to large die size - NEW PROCEDURE.<br>(2)Prior to build: Contractor planned to usc a low-temperature solder - NEW PROCEDURE. Use of solder had been requested by JPL. Contractor said the unit would not sec higher temperatures later. | (1) These flight spares were not used. - Recommendation: QA review production documentation & qualification of new processes prior to the manufacture of flight hardware,<br>(2) J] 'l, reviewed process documentation & found that the units would subsequently encounter temperatures higher than the melting point of the low temperature solder. Contractor ended up using conductive epoxy. | DQA # 9s- 230 |
| Cassini Flight Computer | Solder joint FAILURES found on main flight computer stacks. Units made in Japan, should have been made in USA. Adhesive not consistently applied. Stack tilted & fractured solder joint, Prototype level. No inspection of parts at contractor prior to" use. | Corrective actions can ied out by contractor<br>-replacement devices made at US plant<br>-uniform application of adhesives<br>-qualified parts<br>-100% inspection of parts prior to use | DQA # 94-078 (Ref. 2) |
| Cassini Solid State Power Switch | Processes reviewed as part of SURVEY prior to build. Some problems with glass seal cracking/damage. | Issues worked prior to build. | resol WI @ mgmnt reviews |
| Pathfinder Converters | Many problems from survey through delivery.<br>(1) SURVEY: JPL identified fact that roll seam welder, although planned for use on JPL build, was not currently in use & no experienced operator was employed at the plant - RE-ACTIVATED PROCESS.<br>(2) FAILURES - cracked capacitors at bottom of stacked chip capacitors.<br>(3) Part intended for failure analysis of anomalous behavior was burnt up in oven, Specification for setting oven temp was written for Fahrenheit. Oven could be set for either F or C. Operator mistakenly set oven to Celsius. | (1) Contractor used solder seal method instead,<br>(2) Rebuilt parts, adding stress relief& used epoxy to bond to board rather than solder,<br>(3) Procedure for ovens re-written. | (Ref. 3)<br>(Ref. 4)<br>(Ref. 5) |
| Cassini Shunt Radiator for RTGs | HISTORY of electrical opens or weak weld joints on Voyager, Galileo and Mars Observer.<br>1) Contractor's pull-test equipment jury rigged-introduces operator variables into tests.<br>2) Up to 7470 difference in weld strengths between different layers of welds.<br>3) One normal looking wc]d fell apart duc to no plating on back side of ribbon wire. | (1) Contractor produced weld samples. JPL hybrid lab tested samples.<br>(2) Contractor adjusted weld schedules to produce consistent strength welds,<br>(3) J} 'l, recommended thorough inspection of ribbon wires prior to welding. | (Ref. 6) |
| Cassini Engine Gimbal Actuator Motor Commutatr Welds | PROJECT CONCERNS led to process review, Stripping, staking, swaging & weld operations:<br>1) Some wires reduced in width try 30% at stripping,.<br>2) Poor weld operation-no heat to wire, all to slot<br>3) Consistency, controls of operations were poor. | (1) Contractor, with JPL help, wrote wire strip procedure - none existed previously.<br>(2) Another contractor performed laser weld,<br>(3) With JPL guidance, contractor improved controls on staking and swaging operations. | (Ref. 7)<br>(Ref. 8) |

DQA 01 SQA = Quality Assurance memo number

## 3.0 Tradeoffs

**The** manufacturing process review tradeoff considers the cost of performing the review versus the potential impact to Project or Experiment in the event of failure, and increased cost and schedule delays duc to preventable rework ant] requalification requirements.

Reviews clone at the time of contractor survey, especiall y before the contract has been awarded, will yield the greatest benefits in terms of early notification and least schedule impact, More and more, JPL is awarding fixed price rather than cost plus type contracts. Prim to contract award, process review of bidders with questionable manufacturing practices and uncontrolled processes will afford JPL timel y opportunit y to negotiate corrections or take an alternate approach to the procurement. This is especiall y important with fixed price contracts where post-award changes to a contract can be very costly. Cost and schedule savings can also be expected when a better vendor is selected. Pre-Award process review for fixed price contracts offer opportunities to contain cost within the contract and identify hidden costs of JPL contract oversight.

Process reviews initiated by the project before start of production in response to project concerns will probably have a good payoff in terms of identifying issues before the parts/systems are built. These reviews, when done shortly prior to initiation of production, have one advantage over a review done prior to contract award in that there is less time for process drift to occur.

Process reviews performed after a problem occurs are more of a failure analysis. 'l'hey can help ident ify the cause of the failure or problem and aid in prevention of simi lar problems in the next lot.

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## 6.0 Acknowledgment


Phi] Barela, Steve Bolin, Joc Bott and John Rice contributed to and/or reviewed this document.

# 16. Problem/Failure Process

## 1.0 Objectives

Avoid recurrence of failures in flight that have occurred in ground testing. Provide corporate memory.

## 2.0 Typical Requirements

Implement a formal Problem/Failure Reporting (P/FR) system applicable to qualification and flight hard ware and soft ware. P/FRs are normally initiated at the first application of power starting at board level testing and continues during higher level of assembly and testing through system and flight.

### 2.1 Rationale

The formal P/FR approach provides a systematic way of documenting; and verifying, analyzing, risk rating, and providing rigorous corrective action to minimize the likelihood of recurrence of the problem. Further, for those problems that arc rated high risk (i .e., significant impact on the mission and some uncertainty about the corrective action, thus rated "Red Flag"), project management (PM) can participate in the P/FR closure process. If PM considers the risk too high, additional resources may be appl ied to reduce the likelihood or severit y of that **risk.**

#### 2.1.1 Relevant Failure Modes

**This** preventative measure is equally effective against all possible failure modes, but does not specifically avoid any particular one.

#### 2.1.2 Supporting Data

Formal P/FR systems have direct benefits to a specific project in the form of identifying mission risk issues associated with problems found during ground testing. There is also an indirect benefit to that same project derived from the P/FR records of prior projects. The indirect benefit has several forms, including: 1 ) searchable P/FR databases on prior programs and 2) reports on P/FR trends etc., on past projects. One such report (JPL D-13482), dealing with in-flight "parts-related" problems revealed that about half of the in-flight problems have been previously manifested during ground testing. Still another such report (JPL D-11383), dealing with "Uplink/Downlink" anomalies, concluded three anomalies related to the uplink/downlink process that occurred in-flight had previously occurred during ground tests, but at least two of these were discounted as having minor potential effect in-flight. The most significant finding of the later study was that five of the six JPL spacecraft studied would have experienced a catastrophic failure of the uplink and/or downlink, if not for designed-in redundancy. Both of these reports point out the extreme importance of understanding the "Physics of Failure" of the ground test problems if in-flight problems are to be avoided. This point will be especiall y critical in the Faster, Better, Cheaper (FBC) programs where cost constraints will tend to drive the projects to single string (non-redundant) hardware designs.

A third study (JPL D- 127'71 ), entitled "Correlation of the Magellan Flight PFR History with Ground-test Results", observed that JPL needs to work closely with system contractors to assure that problems encountered during spacecraft development are adequatel y addressed and ri gorous corrective actions arc implemented. 1.ikewisc, the system contractors need to do the same with their subcontractors and suppliers.

The future FBC environment, combining pressure for single string designs and development by system contractor, makes the above conclusions and observations even more critical for the success of their missions.

## 2.2 Methods

For some time the P/FR system has been transitioning from a "paper" system to a fully functional windows/MAC computer-based system available to all JPL employees. Any onc observing an unexpected event or problem with hardware or software can initiate a P/FR. The problem symptoms are described in as much detail as possible at the time the event occurs. As the problem is anal yzed, the descript ion and root cause of the problem can more accurate] y bc ident i fied. once the problem is properly identified and analyzed, the appropriate corrective action can bc defined and implemented. After this is completed the P/FR can bc closed by appropriate technical and management signatures. All of the above process steps arc documented in the. P/FR computer database that is continuously available to project and laboratory personnel from the time of initiation.

## 3.0 **Tradeoffs**

As with any mitigation process, the cost of implementation versus the avoided cost of future failures is balanced. History has clearly demonstrated that the benefits of the formal P/FR system greatl y outweigh the implementation cost, so there is no question about the need for the P/FR system. The only issue is the implementation details. That is, what hardware and at what point the P/FRs arc written and the rigor used in the analysis and closure of the individual problems.

### 3.1 Effectiveness Versus Failure Modes

As mentioned in section 2. 1.1, the P/FR system does not avoid any specific failure mode, but does reduce the chances of problems experienced in ground testing from recurring later in ground tests and/or during the flight phase of the program. As the test program proceeds and problems occur, and their P/FR worked and properl y closed, the likelihood of recurrence of these particular problems should bc significantly lower because of the awareness of prior problem and its corrective action. As with any of the many failure prevention processes, the P/FR system is not 100% effective. The success of a project's P/FR system is a function of many factors, including resources (i ,c., people & dollars) that can be applied to resolut ion of the problems and schedule slack available for these resolutions. A not hcr important factor is t he accuracy of risk judgments associated with each problem.

### 3.2 **Sensitivities**

The effectiveness (E) of individual P/FR parameters (P) in preventing future failures of the same or related t ypes, for several failure detection levels, is depicted in 'J'able 1. The cost function (p) is also depicted for each P/FR parameter.

"1'able 1: Problem/Failure Process Parameter Sensitivity

| Control Parameters (1') | Effectiveness (E) vs Failure Modes (generic, specific) for default parameter | Parametric Sensitivity dE/dP) [E = Effectiveness of individual P/FR Parameters (1') 'in Preventing future Failures of the Same or Related 1 ypes.] + more eff for param increase 0 neutral - less eff for param increase | | | | | | | | | | | | | | | | | | Cost Function p) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | AVH | SP | HT | HL | CPC | 24H | LTS | OPP | PD | VA | CA | HID | HD | OTC | CC | RR | SR | PDR | PRS | |
| Automated Versus Hard copy System (AVH) | Failure Detection Level | | | | | | | | | | | | | | | | | | | | |
| Starting Point for Failure Reporting (SP) | -Failure Detectable at Board Level, but not at Box Level/ Vice Versa | + /+ | + /0 | 0 /0 | + /0 | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | AVH = + SP = + HT = + HL = + CPC = - 24H = 0 |
| H/W Types Subjected to Failure Reporting (HT) | | | | | | | | | | | | | | | | | | | | | |
| H/W Level Subjected to Failure Reporting (III.) | | | | | | | | | | | | | | | | | | | | | |
| Concurrent P/FR Closure (CPC) | -Failure Detectable at Box Level, but not at Subsys Level/ Vice Versa | + /+ | + /0 | 0 /0 | + /0 | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | LTS = + OPP = 0 PD = + VA = + CA = + |
| 24 Hr Initiation of P/FR (2411) | | | | | | | | | | | | | | | | | | | | | |
| Pass Reqm't to Lower Tier Suppliers (1.1's) | | | | | | | | | | | | | | | | | | | | | |
| one Problem Per P/FR (0111) | -Failure Detectable at Subsys Level, but not at System Level/ Vice Versa | + /+ | + /0 | 0 /0 | + /0 | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | + /+ | HID = 0 HD = + OTC = 0 CC = 0 RR = 0 |
| Problem Description (PD) | | | | | | | | | | | | | | | | | | | | | |
| Verification & Analysis (VA) | | | | | | | | | | | | | | | | | | | | | |
| Corrective Action (CA) | | | | | | | | | | | | | | | | | | | | | |
| H/W Identification (HID) | -Failure Detectable at System Level, but not Inflight | + /+ | + /0 | 0 /0 | + /0 | + /+ | + /0 | + /0 | + /0 | + /0 | + /0 | + /0 | + /0 | + /0 | + /0 | + /0 | + /0 | + /0 | + /0 | + /0 | RR = 0 SR = + PDR = + PRS = + |
| H/W Disposition (HD) | | | | | | | | | | | | | | | | | | | | | |
| Operating Time/Cycles (OTC) | | | | | | | | | | | | | | | | | | | | | |
| Cause Code (CC) | | | | | | | | | | | | | | | | | | | | | |
| Risk Rating (RR) | | | | | | | | | | | | | | | | | | | | | |
| Safety Rating (SR) | | | | | | | | | | | | | | | | | | | | | |
| Part Data, including Part Failure Analysis Report (PDR) | | | | | | | | | | | | | | | | | | | | | |
| Project Review/Signoff (PRS) | | | | | | | | | | | | | | | | | | | | | |

# KEY WORDS